ADVANCE INFORMATION

386™ SL MICROPROCESSOR SuperSet
Highly-Integrated Static 386™ Microprocessor
Complete ISA Peripheral Subsystem
System-Wide Power Management

- **Static 386™ CPU Core**
  - **Runs MS-DOS*, WINDOWS*, OS/2* and UNIX***
  - **Object Code Compatible with Intel 8086, 80286 and 386™ Microprocessors**
- **Architecture Extension for Power Management Transparent to Operating Systems and Applications**
- **Complete ISA System, with Extended Support**
  - **Full ISA Bus Control, Status and Address and Data Interface Logic, with Full 24 mA Drive**
  - **Compatible ISA Bus Peripherals**
  - **System I/O Decoding, Programmable Chip Selects and Support Interfaces**
  - **High-Speed Peripheral Interface Bus (PI-Bus Support)**
  - **New ideaPort Interface for Hardware Expansion**
- **Integrated Cache Controller and Tag RAM**
  - **No-Glue Cache SRAM Interface**
  - **16k, 32k, or 64 kByte Cache Size**
  - **Direct, 2-Way or 4-Way Set Associative Organization**
- **Programmable Memory Control**
  - **No-Glue, Page-Mode DRAM Interface**
  - **SRAM Support for Lowest Power**
  - **512k to 32 MBytes**
  - **Full Hardware LIM EMS 4.0**

The 386™ SL Microprocessor SuperSet combines an ISA bus compatible personal computer's microprocessor, memory controller, cache controller and peripheral subsystems into just two Very Large Scale Integration (VLSI) devices. The product's high-integration and power conservation features reduce the size and power consumption typically associated with fully Industry Standard Architecture (ISA) bus compatible systems. In addition, new expandability and flexibility features offer the capability for continued innovation in battery-operated, space-constrained systems. The SL SuperSet brings 100% ISA-Bus compatibility to system designs ranging from the smallest palm-top and notebook PCs to expandable lap-top systems.

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UNIX is a trademark of AT&T.
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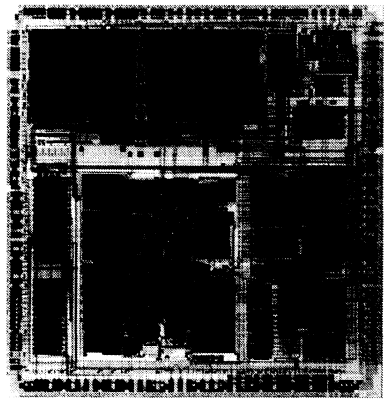

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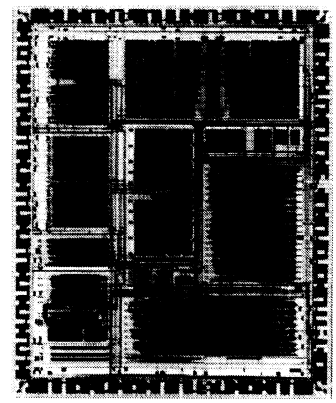

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Figure 1-1. Die Photograph of the 386™ SL Microprocessor (left) and 82360SL ISA Peripheral I/O (right)

386™ SL MICROPROCESSOR
386™ Microprocessor Core, with Integrated Bus Memory, and Cache Controllers; and System Power Management
Fully-Static CHMOS IV Technology

- Static 386™ CPU Core
  - Optimized and Compatible with Standard Operating System Software such as: MS-DOS*, WINDOWS*, OS/2* and UNIX*
  - Object Code Compatible with Intel 8086, 80286 and 386™ Microprocessors
  - Runs All Desk-Top Applications, 16- or 32-Bit
  - D.C. to 20 MHz Operation
  - 32 Megabytes Physical Memory/ 64 Terabytes Virtual Memory
  - 4 Gigabyte Maximum Segment Size
  - High Integration, Low Power Intel CHMOS IV Process Technology
- Transparent Power-Management System Architecture
  - System Management Mode Architecture Extension for Truly Compatible Systems
  - Power Management Transparent to Operating Systems and Application Programs
  - Programmable Hardware Supports Custom Power-Control Methods
- Direct Drive Bus Interfaces
  - Full ISA Bus Interface, with 24 mA Drive
  - High Speed Peripheral Interface Bus
- Integrated Cache Controller and Tag RAM
  - No-Glue Cache SRAM Interface
  - 16k, 32k, or 64 kByte Cache Size
  - Direct, 2-Way or 4-Way Set Associative Organization
  - Write Posting—Double Posted Writes in the Bus Controller
  - 16-Bit Line Size—Reduces Bus Utilization for Cache Line Fills
  - Write-Thru, with SmartHit Algorithm for Reduced Main Memory Power Consumption
- Programmable Memory Control
  - No-Glue, Page-Mode DRAM Interface
  - SRAM Support for Lowest Power
  - 1, 2, or 4 Banks Interleaved, with Programmable Wait States
  - 512k to 32 MBytes
  - Advanced, Flexible Address-Map Configuration
  - Full Hardware LIM EMS 4.0 Address Translation to 32 Megabytes without Waitstate Penalty

82360SL I/O Subsystem
Complete ISA Peripheral Subsystem
Integrated System Power Management
Fully-Static CHMOS IV Technology

- Complete ISA System, with Extended Support
  - — Full ISA Bus Control, Status and Address and Data Interface Logic, with Full 24 mA Drive
  - — Compatible ISA Bus Peripherals:
    - Two 8237 Direct Memory Access Controllers
    - Two 8254 Programmable Timer Counters (6 Timer/Counter Channels)
    - Two 8259A Programmable Interrupt Controllers (15 Channels)
    - Enhanced LS612 Page Memory Mapper
    - One 146818 Real Time Clock w/256-byte CMOS RAM
    - One 16450 Dual Serial Port Controller
    - One 8-Bit Parallel I/O Port (Centronics or Bi-Directional)
  - — Additional System I/O Decoding, Programmable Chip Selects and Support Interfaces:
    - Full Integrated Drive Electronics (I.D.E.) Hard Disk Interface
    - Floppy Disk Controller
- Keyboard Controller Chip Selects and Support Logic
  - — External Real Time Clock Support
  - — PS/2 and EISA Control/Status Ports
  - — Local Memory and ISA-Bus Memory Refresh Control
  - — New ideaPort Interface for Hardware Expansion
- Transparent Power-Management System Architecture
  - — Architecture Extension for Truly Compatible Systems
  - — Transparent to Operating Systems and Applications Programs
  - — Programmable Hardware Supports Custom Power-Control Methods
  - — Integrated Power Management Unit Manages Power-Events Safely

386™ SL Microprocessor SuperSet
386™ SL CPU and 82360SL I/O

1.0 INTRODUCTION

This document provides the pinouts, signal descriptions, and D.C./A.C. electrical characteristics of the 386™SL CPU and 82360SL ISA I/O Peripheral device. Consult Intel for the most recent design-in information. For a thorough description of any functional topic, other than the parametric specifications, please consult the latest 386 SL Microprocessor SuperSet System Design Guide (Order No. 240816), and the 386 SL Microprocessor SuperSet Programmer's Guide (Order No. 240815).

Overview

The 386™SL Microprocessor SuperSet is an extremely flexible pair of components marking a new milestone in microcomputer technology. Included in the pair are a 386 Architecture Central Processing Unit (CPU), several memory subsystem controllers, address translation and remapping logic, an optional cache memory controller, and an extensive collection of ISA bus compatible peripheral functions.

The SL SuperSet allows the personal computer designer to take advantage of the highest level of system integration, while preserving complete freedom in selecting system features, power/performance trade-offs, and value-added enhancements.

Essentially, all of the components needed to build an ISA bus compatible personal computer have been combined within just two components: the 386 SL microprocessor and memory control system, and the 82360SL ISA peripheral I/O and power management subsystem. The only other components needed for a complete personal computer are the main DRAM or optional static memory subsystem, optional cache SRAM and a graphics controller. A minimal amount of commodity Small Scale Integration (SSI) logic or Medium Scale Integration (MSI) logic buffers may be required for design-specific interface to peripheral devices on the ISA bus.

Systems based on the SL SuperSet typically include the functional blocks shown in Figure 1-2.

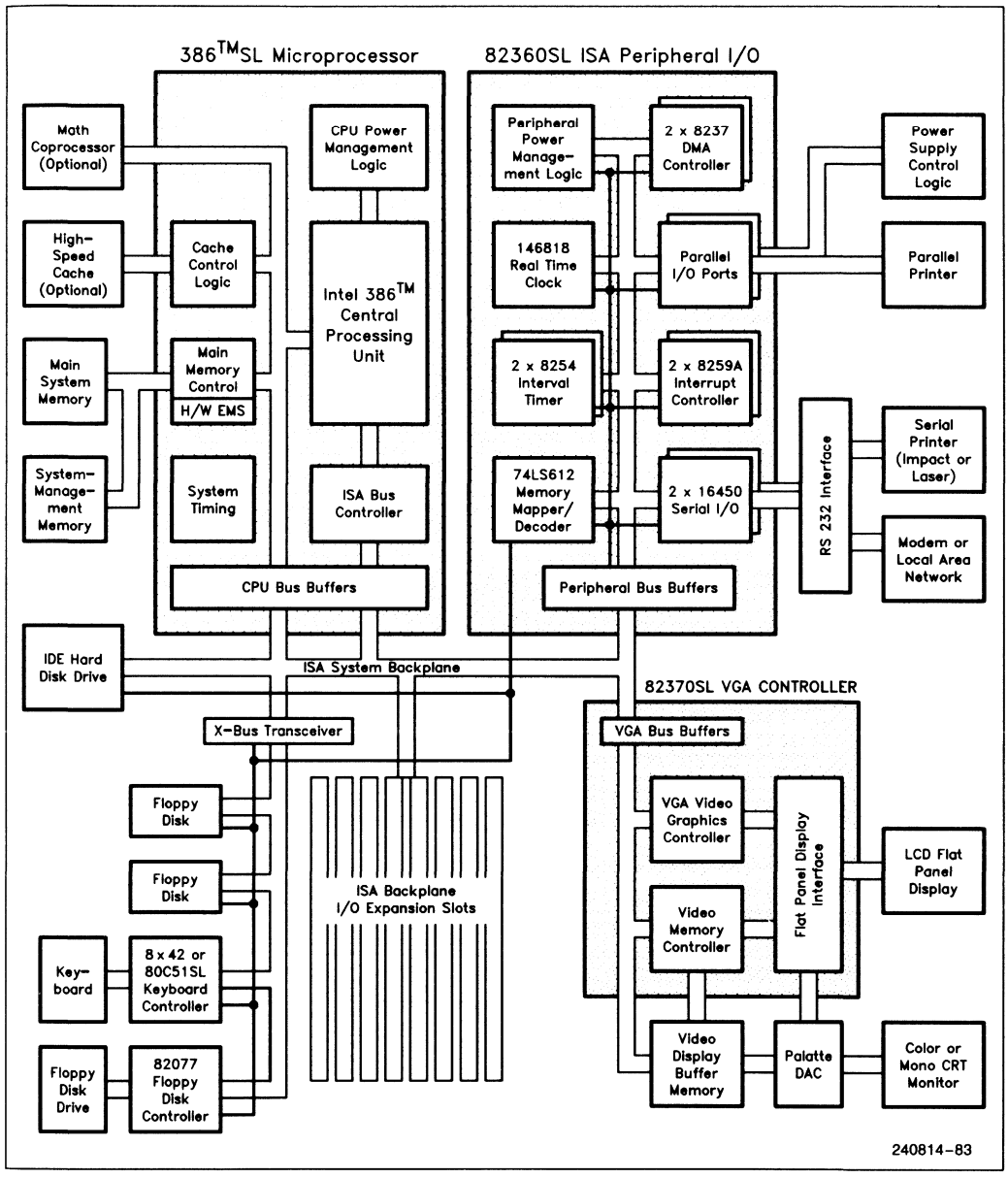


Figure 1-2. 386™SL Microprocessor-Based System Functional Block Diagram

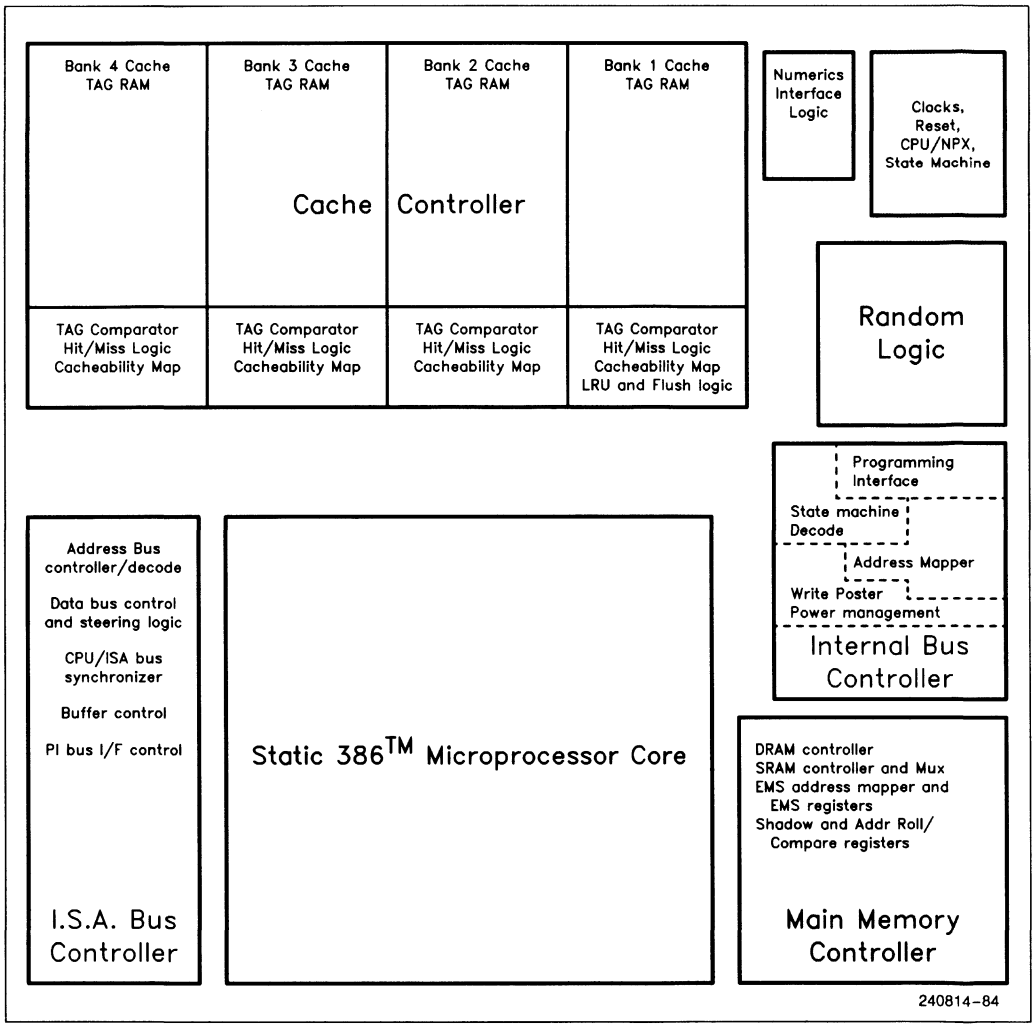


Figure 1-3a. 386™SL Microprocessor Internal Functional Modules

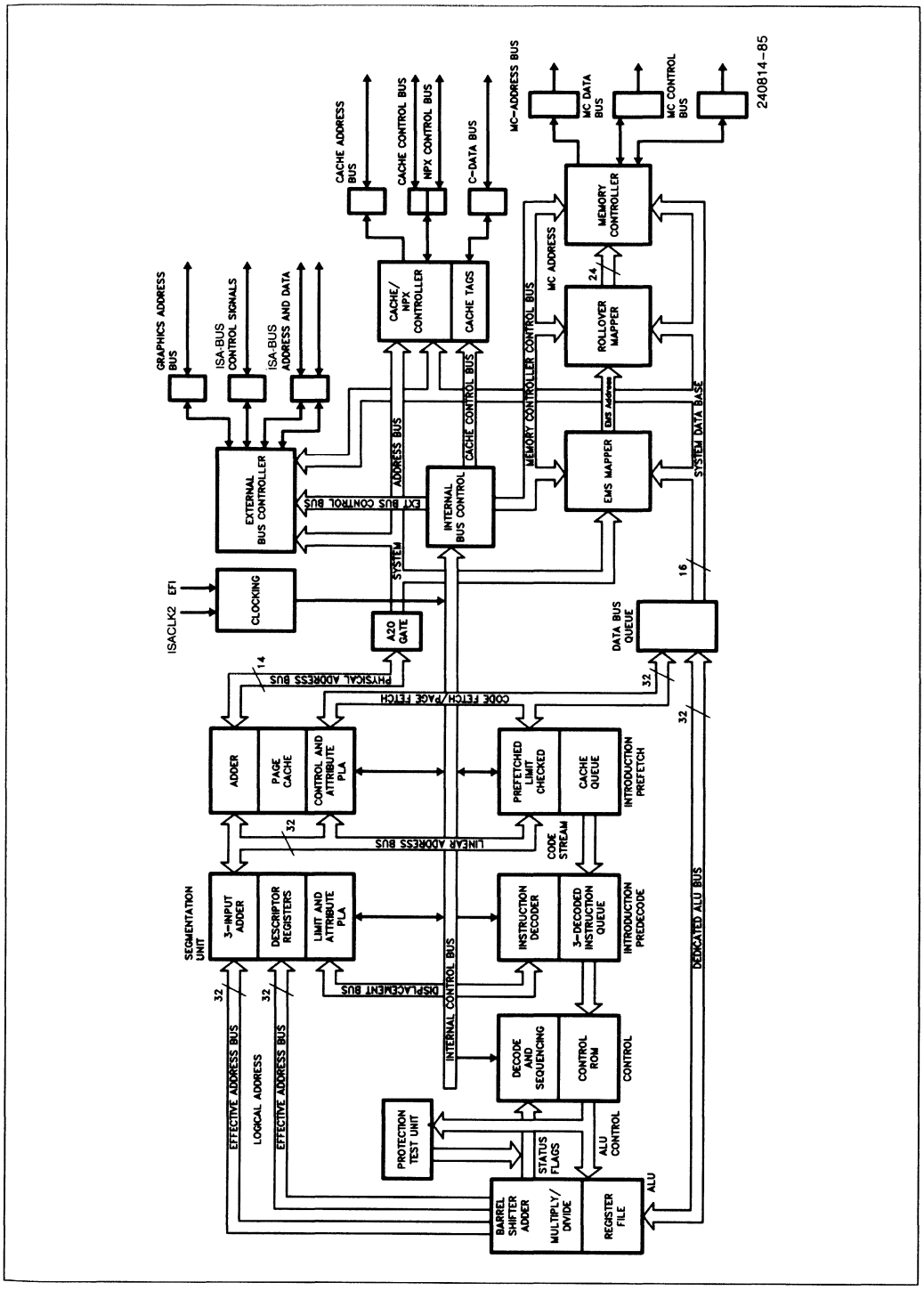


Figure 1-3b. 386™SL Microprocessor Micro-Architecture

386™ SL Microprocessor: Central Processing Unit (CPU) and Memory Controller Subsystem

The 386 SL microprocessor is a highly-integrated, complete microprocessor and memory controller subsystem. At the heart of the 386 SL microprocessor is a CHMOS static 386 CPU core. The 386 CPU core has been fully optimized to reduce run-time power requirements, and includes a key architectural extension required by battery-operated systems.

The 386 SL processor is the first member of the 386 microprocessor product line to implement a CPU with the System Management Mode extension. The System Management Mode is a new CPU operating-mode which allows system vendors to rid their systems of the backwards-compatibility problems that plague battery-operated PCs. This 386 architecture extension eliminates portable-system conflicts by providing a safe, new operating level for the battery management firmware developed by system designers. With the 386™ SL CPU, firmware will execute transparently to every application, operating system and CPU mode, thus avoiding the compatibility conflicts which were once unavoidable.

The 386 SL microprocessor retains the paged-memory-management system, and all other key features which are common to the Intel386™ architecture. In addition, on-chip hardware implements the Expanded Memory Specification (E.M.S.) address translation compatible with the current Lotus/Intel/Microsoft (L.I.M.) E.M.S. 4.0 standard. Additional address-mapping and control logic integrated in the 386 SL CPU allows BIOS ROMs to be "shadowed" by faster memory devices, and supports a variety of common memory roll-over and back-fill schemes. The 386 SL CPU contains all of the control and interface logic needed to directly drive large main memory and an optional cache memory subsystem.

The 386 SL CPU contains bus drivers and control circuitry for two expansion interfaces. A Peripheral Interface Bus (PI-Bus) provides high-speed communication with devices which may reside on the same printed circuit board as the processor. The Industry Standard Architecture (ISA) bus provides a common interface for the wealth of third party ISA bus compatible I/O peripheral and expansion memory add-in boards. On-chip data-byte steering logic, address decoding and mapping logic automatically routes each memory or I/O operation to the appropriate local memory, cache, PI-Bus or ISA expansion bus.

All system configuration logic in the 386 SL processor subsystem is initialized under software control. The system designer only has to program the processor in order to support multiple system hardware designs where many devices of less flexibility were once required. System characteristics such as memory type, size, speed, organization, and mapping; cache size, organization and mapping; and peripheral selection, configuration and mapping are configured under software control. Thereafter, all memory and I/O transfer requests are automatically sent to the appropriate memory space or expansion bus, fully-transparent to existing operating system software and application programs.

Figure 1-3a shows the functional blocks and Figure 1.3b shows the microarchitecture of the 386 SL processor.

82360SL I/O: Integrated ISA Peripheral and Power Management Device

The 82360SL ISA Peripheral I/O contains dedicated logic to perform a number of CPU, memory, and peripheral support functions. The 82360SL device also contains an extensive set of programmable power management facilities which allow minimized system energy requirements for battery-powered portable computers.

The 82360SL includes a complete set of on-chip peripheral device functions including two 16450 compatible serial ports, one 8-bit Centronics interface or bi-directional parallel port, two 8254 compatible timer counters, two 8259 compatible interrupt controllers, two 8237 compatible DMA controllers, one 74LS612 compatible DMA page register, one 146818 compatible Real-time clock/calendar with 256 bytes of battery backed CMOS RAM and an integrated drive electronics (IDE) hard-disk-drive interface. The Intel 82360SL also contains highly programmable chip selects and complete peripheral interface logic for direct keyboard, FLASH memory and floppy disk controller support. The peripheral registers and functions behave exactly as the discrete components commonly found in industry-standard personal computers. The peripheral logic is enhanced for static operation by supporting write only registers as read/write.

The processor and memory support functions contained in the 82360SL device eliminate most of the external random-logic "glue" that might otherwise be required. The 82360SL device provides internal programmable-frequency clock generators for the CPU, backplane, and video subsystems. A programmable, low-power DRAM refresh timer is also provided to maintain system memory integrity during the power saving system stand-by and suspend states.

The 82360SL also contains a flexible set of hardware functions to support the growing sophistication in power management schemes required by portable systems. Numerous hardware timers, event monitors and I/O interfaces can programmably monitor and control system activity. Firmware developed by the system designer allocates and directs the hardware to fulfill the unique power management needs of a given system configuration.

All of the standard peripheral registers, clock-generation logic, and power-management facilities have been designed to ensure complete compatibility with existing operating systems and applications software.

Figure 1-4 shows the functional blocks and microarchitecture of the 82360SL I/O subsystem.

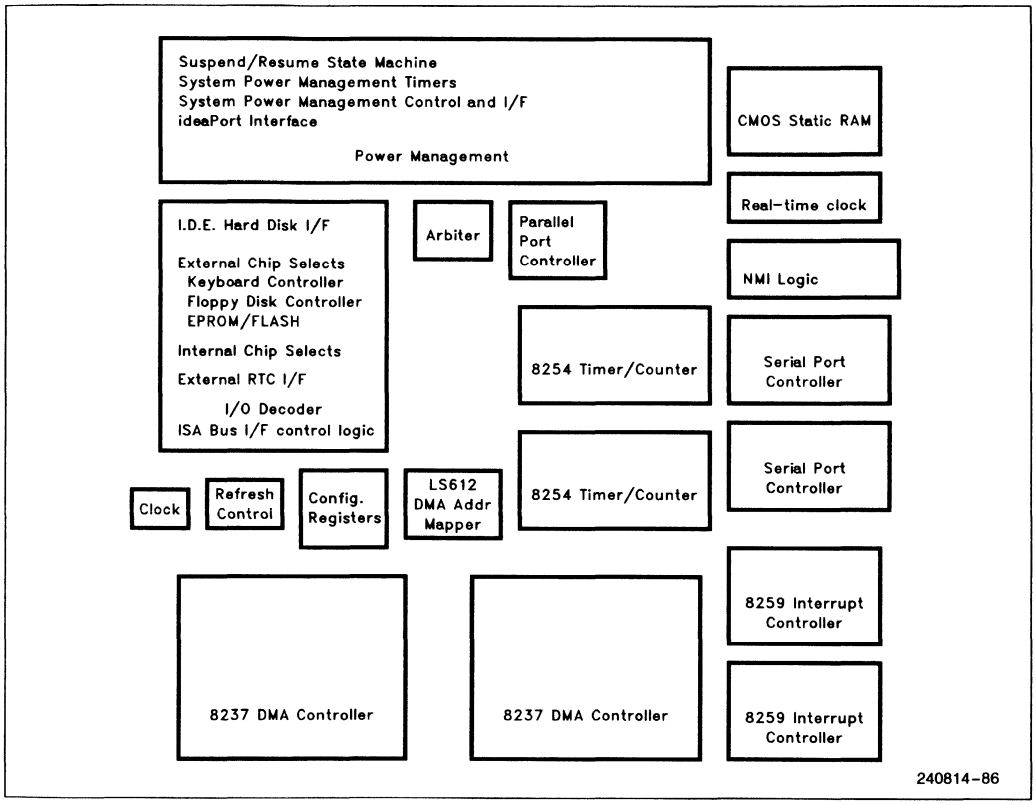


Figure 1-4a. 82360SL ISA Peripheral I/O Internal Functional Modules

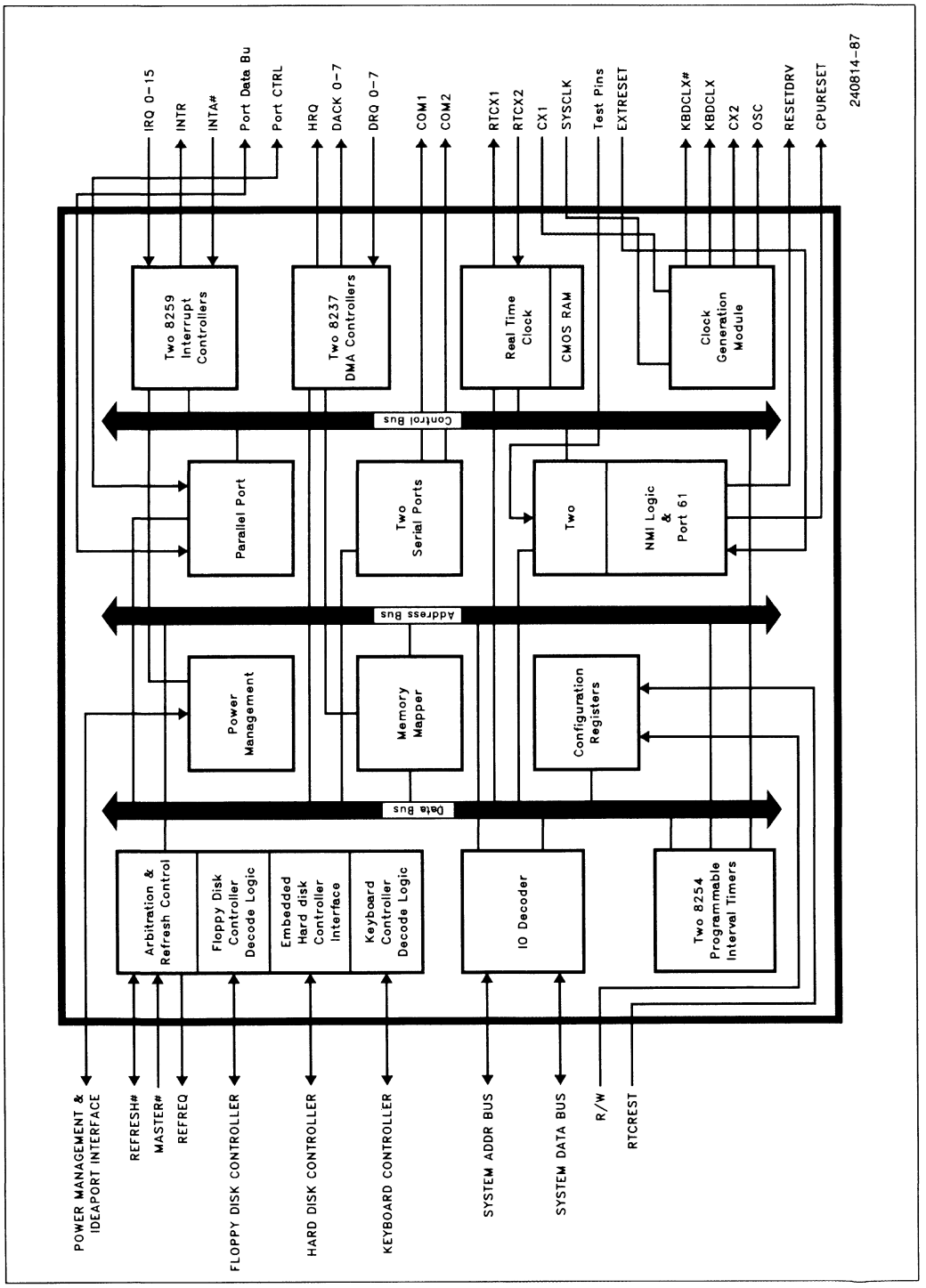


Figure 1-4b. 82360SL Functional Block Diagram

2.0 PIN ASSIGNMENTS AND SIGNAL CHARACTERISTICS

Section 2 provides information for the SL SuperSet pin assignment with respect to the signal mnuemonics. In addition to the package pin out diagrams, two tables are provided for easy location of signals. The first table lists the 386 SL CPU package device pinouts in the 227 pin Land Grid Array (LGA). The second table lists the 82360SL package device pinouts in the 196 lead JEDEC Plastic Quad Flat Package (PQFP). Both tables include additional information for the signals and associated pin numbers. A brief explanation of each column of the table is given in Table 2-1.

Table 2-1. Description of the Columns of Tables 2-2 and 2-3

PQFP	This column lists the pin numbers of the 82360SL in a Plastic Quad Flat Package.
LGA	This column lists the pin numbers of the 386 SL CPU in a Land Grid Array.
Signal Name	This column lists the signal name associated with the package pins.
Type	Indicates whether the pin is an Input (I), an Output (O) or an Input-Output (IO).
Term	Specifies the internal terminator on the pin. This could be an internal pull-up or pull-down resistor value or a hold circuit. To find out whether a pull-up or a pull-down is provided, use the STPCK (Stop Clock) column.
Drive	Specifies the drive current I_{OH} (Current Output Logic High) and I_{OL} (Current Output Logic Low) in milli-Amperes (mA) for output (O), and bi-directional (IO), pins.
Load	This column lists the maximum specified capacitive load which the buffer can directly drive in pico-Farads (pF) for each signal. This is specified for output and input-output pins only.
Susp.	This column specifies the state of the pin during a suspend operation. Input signals have the representation Tri/x where x is either a logic 0 or logic 1. This indicates that the input is internally isolated and that the internal termination on the pin is tri-stated or disabled. When in Suspend Mode an external logic value x is forced to the internal logic. The input can be driven to the same logic HIGH or LOW state by external logic with no current source or sink. The additional output buffer abbreviations are explained below. Tri - Tristated Actv - Active 0 - held low 1 - held high Hold - held at last state
Stpck.	This column specifies the state of the pin when the clock signal CPUCLK is internally stopped in the 386 SL CPU. Pu - Pulled up Pd - Pulled down Drv - Driven high, low or at the last state Actv - Active (Signal is driven and continues to operate or change logic states)
ONCE	This column specifies the state of the pin when the ONCE# (On Circuit Emulator) pin is asserted, allowing in-circuit testing while the device is still populated on the logic board. Tri - Floats Actv - Active 0 - held low 1 - held high Hold - held at last state
Derating Curve	This column specifies which derating curve(1) is used for each output buffer associated with the pin.

NOTE:
1. For more information on derating curves and how to use them, see Section 8 (Capacitive Derating Information).

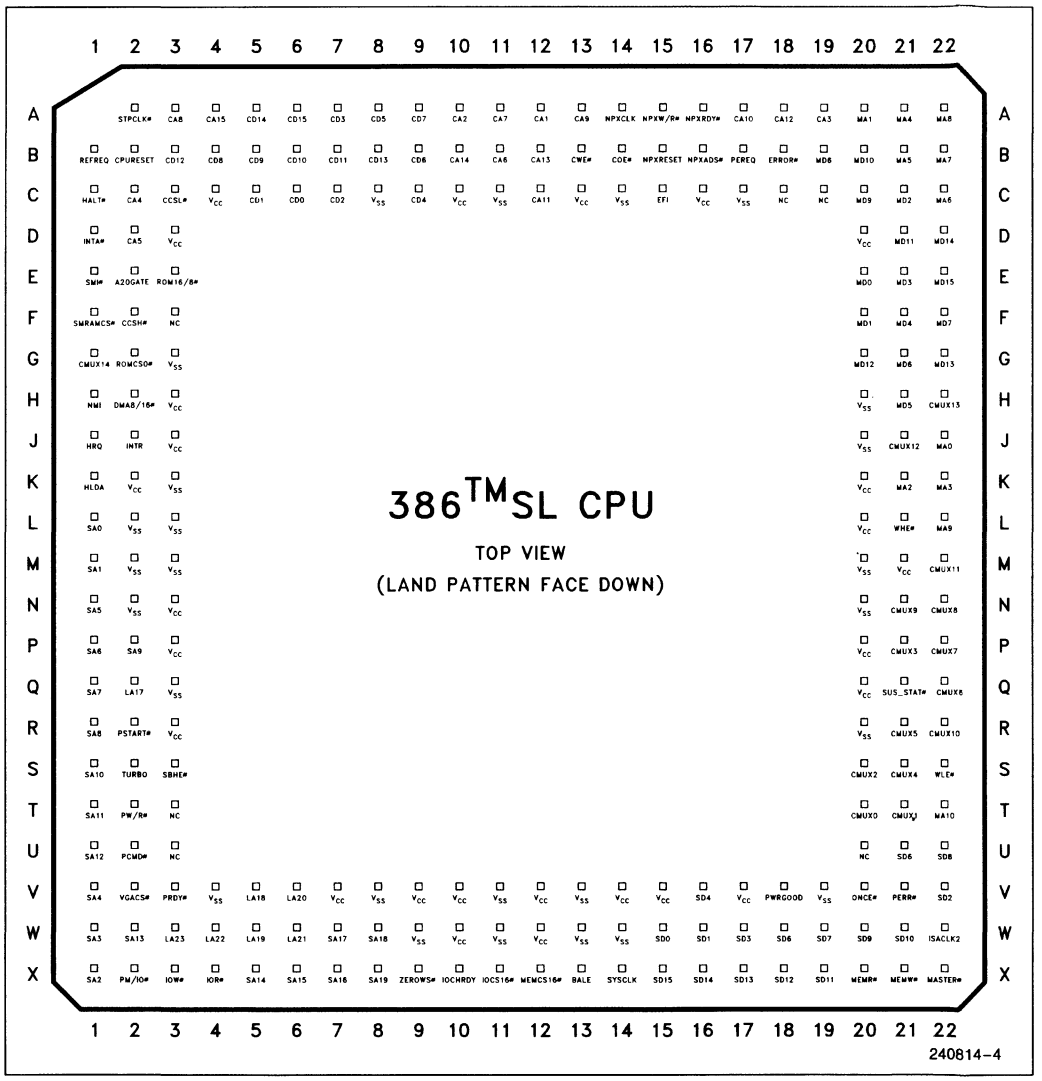


Figure 2-1. Pin Assignments of the 386™ SL CPU in the 227-Lead LGA Package (Top View—Land Pattern Facing Down, Component Marking Facing Up)

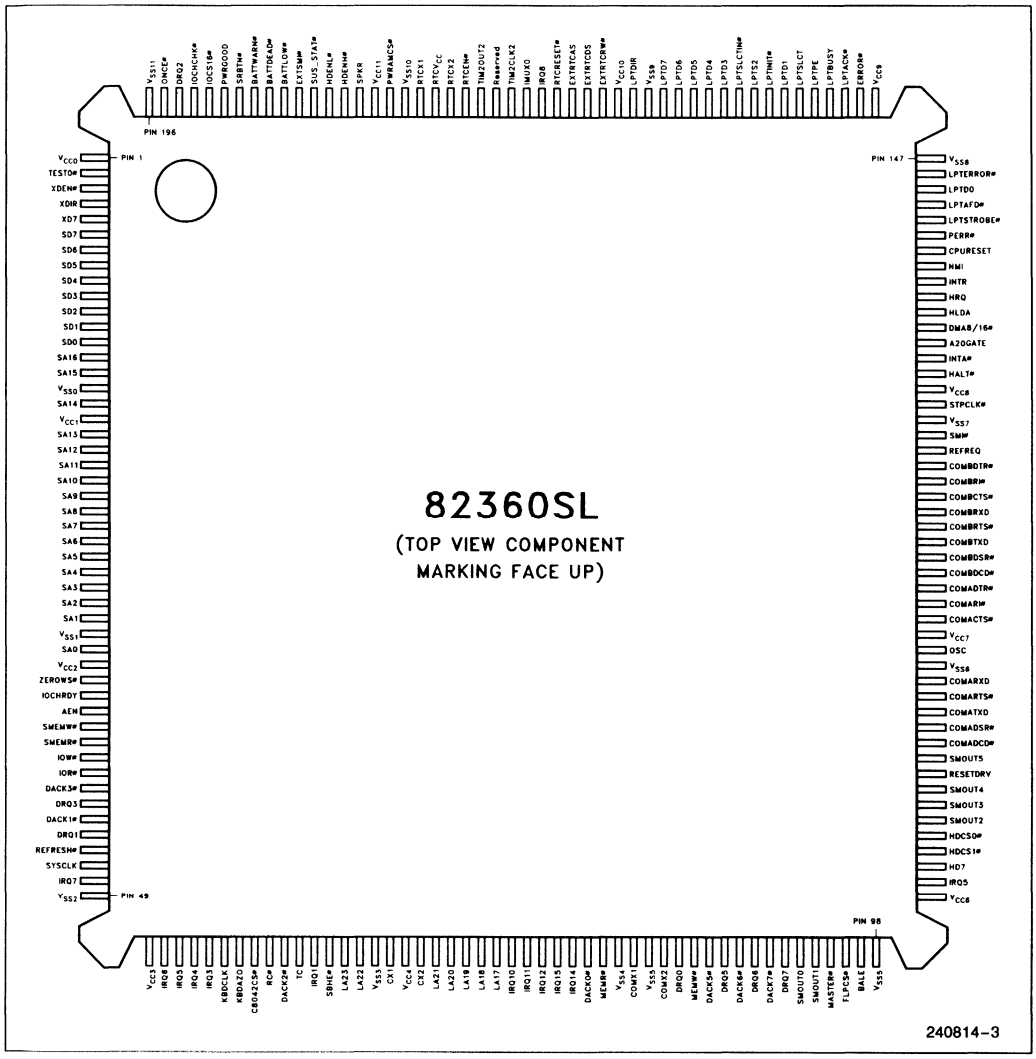


Figure 2-2. Pin Assignments for the 82360SL in a 196-Lead Plastic Quad Flat Package

Table 2-2. 386™SL CPU Pin Characteristics

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
A02	STPCLK#	I	60K			Tri/1	Pu	Tri/1	
A03	CA8	O	Hold	4, 2	45	Hold	Drv	Hold	F
A04	CA15	O	Hold	4, 2	45	Hold	Drv	Hold	F
A05	CD14	IO	Hold	4, 2	50	Hold	Drv	Hold	I
A06	CD15	IO	Hold	4, 2	50	Hold	Drv	Hold	I
A07	CD3	IO	Hold	4, 2	50	Hold	Drv	Hold	I
A08	CD5	IO	Hold	4, 2	50	Hold	Drv	Hold	I
A09	CD7	IO	Hold	4, 2	50	Hold	Drv	Hold	I
A10	CA2	O	Hold	4, 2	60	Hold	Drv	Hold	F
A11	CA7	O	Hold	4, 2	45	Hold	Drv	Hold	F
A12	CA1	O	Hold	4, 2	45	Hold	Drv	Hold	F
A13	CA9	O	Hold	4, 2	45	Hold	Drv	Hold	F
A14	NPXCLK	O	Hold	4, 2	20	Hold	Drv	Hold	F
A15	NPXW/R#	O	Hold	4, 2	30	Hold	Drv	Hold	F
A16	NPXRDY#	I	60K			Tri/1	Pu	Tri/1	
A17	CA10	O	Hold	4, 2	45	Hold	Drv	Hold	F
A18	CA12	O	Hold	4, 2	45	Hold	Drv	Hold	F
A19	CA3	O	Hold	4, 2	45	Hold	Drv	Hold	F
A20	MA1	O	Hold	4, 2	300	Hold	Drv	Hold	E
A21	MA4	O	Hold	4, 2	300	Hold	Drv	Hold	E
A22	MA8	O	Hold	4, 2	300	Hold	Drv	Hold	E
B01	REFREQ	I	Hold			Actv	Actv	Tri/0	
B02	CPURESET	I	20K			Tri/0	Pd	Tri/0	
B03	CD12	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B04	CD8	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B05	CD9	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B06	CD10	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B07	CD11	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B08	CD13	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B09	CD6	IO	Hold	4, 2	50	Hold	Drv	Hold	I
B10	CA14	O	Hold	4, 2	45	Hold	Drv	Hold	F
B11	CA6	O	Hold	4, 2	45	Hold	Drv	Hold	F
B12	CA13	O	Hold	4, 2	45	Hold	Drv	Hold	F

NOTES:
1. Tri/1 indicates a tri-stateable output with pull-up.
2. Tri/0 indicates a tri-stateable output with pull-down.
3. CMUX 8–11 (RASxx#) are ACTIVE when the 386™SL CPU Memory Controller is programmed in the DRAM controller mode with Suspend Refresh enabled. Otherwise, these signals are HOLD.

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
B13	CWE#	O	Hold	4, 2	45	Hold	Drv	Hold	I
B14	COE#	O	Hold	4, 2	45	Hold	Drv	Hold	F
B15	NPXRESET#	O	Hold	4, 2	20	Hold	Drv	Hold	F
B16	NPXADS#	O	Hold	4, 2	30	Hold	Drv	Hold	F
B17	PEREQ	I	20K			Tri/0	Pd	Tri/0	
B18	ERROR#	I	60K			Tri/1	Pu	Tri/1	
B19	MD8	IO	Hold	4, 2	68	Hold	Drv	Hold	H
B20	MD10	IO	Hold	4, 2	68	Hold	Drv	Hold	H
B21	MA5	O	Hold	4, 2	300	Hold	Drv	Hold	E
B22	MA7	O	Hold	4, 2	300	Hold	Drv	Hold	E
C01	HALT#	O	Hold	4, 2	65	Hold	Drv	Hold	G
C02	CA4	O	Hold	4, 2	45	Hold	Drv	Hold	F
C03	CCSL#	O	Hold	4, 2	35	Hold	Drv	Hold	F
C04	V_{CC}								
C05	CD1	IO	Hold	4, 2	50	Hold	Drv	Hold	I
C06	CD0	IO	Hold	4, 2	50	Hold	Drv	Hold	
C07	CD2	IO	Hold	4, 2	50	Hold	Drv	Hold	I
C08	V_{SS}								
C09	CD4	IO	Hold	4, 2	50	Hold	Drv	Hold	I
C10	V_{CC}								
C11	V_{SS}								
C12	CA11	O	Hold	4, 2	45	Hold	Drv	Hold	F
C13	V_{CC}								
C14	V_{SS}								
C15	EFI	I							
C16	V_{CC}								
C17	V_{SS}								
C18	BUSY#	I	60K			Tri/1	Pu	Tri/1	
C19	nc								
C20	MD9	IO	Hold	4, 2	68	Hold	Drv	Hold	H
C21	MD2	IO	Hold	4, 2	68	Hold	Drv	Hold	H
C22	MA6	O	Hold	4, 2	300	Hold	Drv	Hold	E
D01	INTA#	O	Hold	4, 2	65	Hold	Drv	Hold	G

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin#	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
D02	CA5	O	Hold	4, 2	45	Hold	Drv	Hold	F
D03	V_{CC}								
D20	V_{CC}								
D21	MD11	IO	Hold	4, 2	68	Hold	Drv	Hold	H
D22	MD14	IO	Hold	4, 2	68	Hold	Drv	Hold	H
E01	SMI#	I	60K			Tri/1	Pu	Tri/1	
E02	A20GATE	I	20K			Tri/0	Pd	Tri/0	
E03	ROM16/8#	I	60K			Tri/1	Pu	Tri/1	
E20	MD0	IO	Hold	4, 2	68	Hold	Drv	Hold	H
E21	MD3	IO	Hold	4, 2	68	Hold	Drv	Hold	H
E22	MD15	IO	Hold	4, 2	68	Hold	Drv	Hold	H
F01	SMRAMCS#	O	Hold	4, 2	65	Drv	Drv	Hold	G
F02	CCSH#	O	Hold	4, 2	35	Hold	Drv	Hold	F
F03	NC								
F20	MD1	IO	Hold	4, 2	68	Hold	Drv	Hold	H
F21	MD4	IO	Hold	4, 2	68	Hold	Drv	Hold	H
F22	MD7	IO	Hold	4, 2	68	Hold	Drv	Hold	H
G01	CMUX14	O	Hold	4, 2	65	Hold	Drv	Hold	G
G02	ROMCS0#	O	Hold	4, 2	65	Hold	Drv	Hold	G
G03	V_{SS}								
G20	MD12	IO	Hold	4, 2	68	Hold	Drv	Hold	H
G21	MD6	IO	Hold	4, 2	68	Hold	Drv	Hold	H
G22	MD13	IO	Hold	4, 2	68	Hold	Drv	Hold	H
H01	NMI	I	20K			Tri/0	Pd	Tri/0	
H02	DMA8/16#	I	60K			Tri/1	Pu	Tri/1	
H03	V_{CC}								
H20	V_{SS}								
H21	MD5	IO	Hold	4, 2	68	Hold	Drv	Hold	H
H22	CMUX13	IO	Hold	4, 2	68	Hold	Drv	Hold	H
J01	HRQ	I	20K			Tri/0	Pd	Tri/0	
J02	INTR	I	20K			Tri/0	Pd	Tri/0	
J03	V_{CC}								
J20	V_{SS}								

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
J21	CMUX12	IO	Hold	4, 2	68	Hold	Drv	Hold	H
J22	MA0	O	Hold	4, 2	300	Hold	Drv	Hold	E
K01	HLDA	O	Hold	4, 2	65	Hold	Drv	Hold	G
K02	V_{CC}								
K03	V_{SS}								
K20	V_{CC}								
K21	MA2	O	Hold	4, 2	300	Hold	Drv	Hold	E
K22	MA3	O	Hold	4, 2	300	Hold	Drv	Hold	E
L01	SA0	IO	Hold	24, 4	240	Hold	Drv	Hold	C
L02	V_{SS}								
L03	V_{SS}								
L20	V_{CC}								
L21	WHE#	O	Hold	4, 2	300	Tri/1	Drv	Hold	D
L22	MA9	O	Hold	4, 2	300	Hold	Drv	Hold	E
M01	SA1	IO	Hold	24, 4	240	Hold	Drv	Hold	C
M02	V_{SS}								
M03	V_{SS}								
M20	V_{SS}								
M21	V_{CC}								
M22	CMUX11	O	Hold	4, 2	144	Actv(3)	Drv	Hold	A
N01	SA5	IO	Hold	24, 4	240	Hold	Drv	Hold	C
N02	V_{SS}								
N03	V_{CC}								
N20	V_{SS}								
N21	CMUX9	O	Hold	4, 2	144	Actv(3)	Drv	Hold	A
N22	CMUX8	O	Hold	4, 2	144	Actv(3)	Drv	Hold	A
P01	SA6	IO	Hold	24, 4	240	Hold	Drv	Hold	C
P02	SA9	IO	Hold	24, 4	240	Hold	Drv	Hold	C
P03	V_{CC}								
P20	V_{CC}								
P21	CMUX3	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
P22	CMUX7	O	Hold	4, 2	72	Hold	Drv	Hold	H
Q01	SA7	IO	Hold	24, 4	240	Hold	Drv	Hold	C

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
Q02	LA17	IO	Hold	24, 4	240	Hold	Drv	Hold	C
Q03	V_{SS}								
Q20	V_{CC}								
Q21	SUS_STAT#	I	60K			Actv	Actv	Tri/1	
Q22	CMUX6	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
R01	SA8	IO	Hold	24, 4	240	Hold	Drv	Hold	C
R02	PSTART#	O	Hold	4, 2	65	Hold	Drv	Hold	G
R03	V_{CC}								
R20	V_{SS}								
R21	CMUX5	O	Hold	4, 2	72	Tri/1	Drv	Hold	H
R22	CMUX10	O	Hold	4, 2	144	Actv(3)	Drv	Hold	A
S01	SA10	IO	Hold	24, 4	240	Hold	Drv	Hold	C
S02	TURBO	I	60K			Tri/1	Pu	Tri/1	
S03	SBHE#	IO	Hold	24, 4	240	Hold	Drv	Hold	C
S20	CMUX2	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
S21	CMUX4	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
S22	WLE#	O	Hold	4, 2	300	Tri/1	Drv	Hold	D
T01	SA11	IO	Hold	24, 4	240	Hold	Drv	Hold	C
T02	PW/R#	O	Hold	4, 2	65	Hold	Drv	Hold	G
T03	NC								
T20	CMUX0	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
T21	CMUX1	O	Hold	4, 2	72	Tri/0	Drv	Hold	H
T22	MA10	O	Hold	4, 2	300	Hold	Drv	Hold	E
U01	SA12	IO	Hold	24, 4	240	Hold	Drv	Hold	C
U02	PCMD#	O	Hold	4, 2	65	Hold	Drv	Hold	G
U03	NC								
U20	NC								
U21	SD5	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
U22	SD8	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
V01	SA4	IO	Hold	24, 4	240	Hold	Drv	Hold	C
V02	VGACS#	O	Hold	4, 2	65	Hold	Drv	Hold	G
V03	PRDY#	I	60K			Tri/1	Pu	Tri/1	

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
V04	V_{SS}								
V05	LA18	IO	Hold	24, 4	240	Hold	Drv	Hold	C
V06	LA20	IO	Hold	24, 4	240	Hold	Drv	Hold	C
V07	V_{CC}								
V08	V_{SS}								
V09	V_{CC}								
V10	V_{CC}								
V11	V_{SS}								
V12	V_{CC}								
V13	V_{SS}								
V14	V_{CC}								
V15	V_{CC}								
V16	SD4	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
V17	V_{CC}								
V18	PWRGOOD	I				Actv	Actv	Tri/0	
V19	V_{SS}								
V20	ONCE#	I	60K			Tri/1	Pu	Actv	
V21	PERR#	O	Hold	4, 2	68	Hold	Drv	Hold	H
V22	SD2	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W01	SA3	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W02	SA13	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W03	LA23	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W04	LA22	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W05	LA19	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W06	LA21	IO	Hold	24, 4	240	Hold	Drv	Hold	C
W07	SA17	O	Hold	24, 4	240	Hold	Drv	Hold	C
W08	SA18	O	Hold	24, 4	240	Hold	Drv	Hold	C
W09	V_{SS}								
W10	V_{CC}								
W11	V_{SS}								
W12	V_{CC}								
W13	V_{SS}								
W14	V_{SS}								

Table 2-2. 386™SL CPU Pin Characteristics (Continued)

LGA Pin #	Signal Name	Type	Term	Drive	Load	Susp	Stpck	ONCE	Derating Curve
W15	SD0	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W16	SD1	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W17	SD3	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W18	SD6	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W19	SD7	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W20	SD9	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W21	SD10	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
W22	ISACLK2	I							
X01	SA2	IO	Hold	24, 4	240	Hold	Drv	Hold	C
X02	PM/IO#	O	Hold	4, 2	65	Hold	Drv	Hold	G
X03	IOW#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	B
X04	IOR#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	B
X05	SA14	IO	Hold	24, 4	240	Hold	Drv	Hold	C
X06	SA15	IO	Hold	24, 4	240	Hold	Drv	Hold	C
X07	SA16	IO	Hold	24, 4	240	Hold	Drv	Hold	C
X08	SA19	O	Hold	24, 4	240	Hold	Drv	Hold	C
X09	ZEROWS#	I	300			Tri/1	Pu	Tri/1	
X10	IOCHRDY	IO	300	24, 4	240	Tri/1	Pu	Tri/1	D
X11	IOCS16#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X12	MEMCS16#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X13	BALE	O	Hold	24, 4	240	Hold	Drv	Hold	D
X14	SYSCLK	O	Hold	4, 2	120	Hold	Drv	Hold	G
X15	SD15	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X16	SD14	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X17	SD13	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X18	SD12	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X19	SD11	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	D
X20	MEMR#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	B
X21	MEMW#	IO	60K	24, 4	240	Tri/1	Pu	Tri/1	B
X22	MASTER#	I	60K			Tri/1	Pu	Tri/1	

Table 2-3. 82360SL Pin Characteristics

PQFP Pin #	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B1	V_{CC}							
B2	TESTO#	I	60K			Tri	Pu	
B3	XDEN#	O		12	50	Tri	Tri	M
B4	XDIR	O		12	50	Tri	Tri	M
B5	XD7	IO	60K	24	100	Tri	Tri/1	J
B6	SD7	IO		24	240	Tri	Tri	J
B7	SD6	IO		24	240	Tri	Tri	J
B8	SD5	IO		24	240	Tri	Tri	J
B9	SD4	IO		24	240	Tri	Tri	J
B10	SD3	IO		24	240	Tri	Tri	J
B11	SD2	IO		24	240	Tri	Tri	J
B12	SD1	IO		24	240	Tri	Tri	J
B13	SD0	IO		24	240	Tri	Tri	J
B14	SA16	IO		24	240	Tri	Tri	J
B15	SA15	IO		24	240	Tri	Tri	J
B16	V_{SS}							
B17	SA14	IO		24	240	Tri	Tri	J
B18	V_{CC}							
B19	SA13	IO		24	240	Tri	Tri	J
B20	SA12	IO		24	240	Tri	Tri	J
B21	SA11	IO		24	240	Tri	Tri	J
B22	SA10	IO		24	240	Tri	Tri	J
B23	SA9	IO		24	240	Tri	Tri	J
B24	SA8	IO		24	240	Tri	Tri	J
B25	SA7	IO		24	240	Tri	Tri	J
B26	SA6	IO		24	240	Tri	Tri	J
B27	SA5	IO		24	240	Tri	Tri	J
B28	SA4	IO		24	240	Tri	Tri	J
B29	SA3	IO		24	240	Tri	Tri	J
B30	SA2	IO		24	240	Tri	Tri	J
B31	SA1	IO		24	240	Tri	Tri	J
B32	V_{SS}							

Table 2-3. 82360SL Pin Characteristics (Continued)

PQFP Pin #	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B33	SA0	IO		24	240	Tri	Tri	J
B34	V_{CC}							
B35	ZEROWS#	OD		24	240	Tri	Tri	K
B36	IOCHRDY	OD		24	240	Tri	Tri	K
B37	AEN	O		24	240	Tri	Tri	K
B38	SMEMW#	O	60K	24	240	Tri	Tri	K
B39	SMEMR#	O	60K	24	240	Tri	Tri	K
B40	IOW#	IO		24	240	Tri	Tri	K
B41	IOR#	IO		24	240	Tri	Tri	K
B42	DACK3#	O		12	50	Tri	Tri	M
B43	DRQ3	I	20K			Pd	Pd	
B44	DACK1#	O		12	50	Tri	Tri	M
B45	DRQ1	I	20K			Pd	Pd	
B46	REFRESH#	OD	300	16	240	Tri	Pu	K
B47	SYSCLK	I	100K			Pd	Pd	
B48	IRQ7	I	10K			Tri	Pu	
B49	V_{SS}							
B50	V_{CC}							
B51	IRQ6	I	10K			Tri	Pu	
B52	IRQ5	I	10K			Tri	Pu	
B53	IRQ4	I	10K			Tri	Pu	
B54	IRQ3	I	10K			Tri	Pu	
B55	KBDCLK	O		12	50	Tri	Tri	M
B56	KBDA20	I	20K			Pd	Pd	
B57	C8042CS#	O		12	50	Tri	Tri	M
B58	RC#	I	60K			Tri	Pu	
B59	DACK2#	O		12	50	Tri	Tri	M
B60	TC	O		24	240	Tri	Tri	K
B61	IRQ1	I	10K			Tri	Pu	
B62	SBHE#	O		24	240	Tri	Tri	K
B63	LA23	IO		24	240	Tri	Tri	J
B64	LA22	IO		24	240	Tri	Tri	J
B65	V_{SS}							

Table 2-3. 82360SL Pin Characteristics (Continued)

PQFP Pin #	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B66	CX1	I					Actv	
B67	V_{CC}							
B68	CX2	O					Actv	
B69	LA21	IO		24	240	Tri	Tri	J
B70	LA20	IO		24	240	Tri	Tri	J
B71	LA19	IO		24	240	Tri	Tri	J
B72	LA18	IO		24	240	Tri	Tri	J
B73	LA17	IO		24	240	Tri	Tri	J
B74	IRQ10	I	10K			Tri	Pu	
B75	IRQ11	I	10K			Tri	Pu	
B76	IRQ12	I	10K			Tri	Pu	
B77	IRQ15	I	10K			Tri	Pu	
B78	IRQ14	I	10K			Tri	Pu	
B79	DACK0#	O		12	50	Tri	Tri	M
B80	MEMR#	IO		24	240	Tri	Tri	K
B81	V_{SS}							
B82	COMX1	I					Actv	
B83	V_{CC}							
B84	COMX2	O					Actv	
B85	DRQ0	I	20K			Pd	Pd	
B86	MEMW#	IO		24	240	Tri	Tri	K
B87	DACK5#	O		12	50	Tri	Tri	M
B88	DRQ5	I	20K			Pd	Pd	
B89	DACK6#	O		12	50	Tri	Tri	M
B90	DRQ6	I	20K			Pd	Pd	
B91	DACK7#	O		12	50	Tri	Tri	M
B92	DRQ7	I	20K			Pd	Pd	
B93	SMOUT0	O		12	50	Tri	Tri	M
B94	SMOUT1	O		12	50	Tri	Tri	M
B95	MASTER#	I				Tri	Tri	
B96	FLPCS#	O		12	50	Tri	Tri	M
B97	BALE	I	100K			Pd	Pd	
B98	V_{SS}							
B99	V_{CC}							
B100	IRQ9	I	10K			Tri	Pu	

Table 2-3. 82360SL Pin Characteristics (Continued)

PQFP Pin #	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B101	HD7	IO	60K	24	100	Tri	Tri/1	J
B102	HDCS1#	O		12	50	Tri	Tri	M
B103	HDCS0#	O		12	50	Tri	Tri	M
B104	SMOUT2	O		12	50	Tri	Tri	M
B105	SMOUT3	O		12	50	Tri	Tri	M
B106	SMOUT4	O		12	50	Tri	Tri	M
B107	RESETDRV	O		24	240	Tri	Tri	K
B108	SMOUT5	O		12	50	Tri	Tri	M
B109	COMADCD#	I	60K			Tri	Pu	
B110	COMADSR#	I	60K			Tri	Pu	
B111	COMATXD	O		12	50	Tri	Tri	M
B112	COMARTS#	O		12	50	Tri	Tri	M
B113	COMARXD	I	20K			Pd	Pd	
B114	V_{SS}							
B115	OSC	O		24	240	Tri	Tri	K
B116	V_{CC}							
B117	COMACTS#	I	60K			Tri	Pu	
B118	COMARI#	I	60K			Actv	Pu	
B119	COMADTR#	O		12	50	Tri	Tri	M
B120	COMBDCD#	I	60K			Tri	Pu	
B121	COMBDSR#	I	60K			Tri	Pu	
B122	COMBTXD	O		12	50	Tri	Tri	M
B123	COMBRTS#	O		12	50	Tri	Tri	M
B124	COMBRXD	I	20K			Pd	Pd	
B125	COMBCTS#	I	60K			Tri	Pu	
B126	COMBRI#	I	60K			Actv	Pu	
B127	COMBDTR#	O		12	50	Tri	Tri	M
B128	REFREQ	O		12	50	Actv(1)	Actv	M
B129	SMI#	O		12	50	Tri	Tri	M
B130	V_{SS}							
B131	STPCLK#	O		12	50	Tri	Tri	M
B132	V_{CC}							

NOTE:
1. Programmable, active only when suspend refresh is enabled.

Table 2-3. 82360SL Pin Characteristics (Continued)

PQFP Pin #	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B133	HALT#	I	60K			Tri	Pu	
B134	INTA#	I	60K			Tri	Pu	
B135	A20GATE	O		12	50	Tri	Tri	M
B136	DMA8/16#	O		12	50	Tri	Tri	M
B137	HLDA	I	20K			Pd	Pd	
B138	HRQ	O		12	50	Tri	Tri	M
B139	INTR	O		12	50	Tri	Tri	M
B140	NMI	O		12	50	Tri	Tri	M
B141	CPURESET	O		12	50	Tri	Tri	M
B142	PERR#	I	60K			Tri	Pu	
B143	LPTSTROBE#	OD	4K7	12	100	Tri	Tri	L
B144	LPTAFD#	OD	4K7	12	100	Tri	Tri	L
B145	LPTD0	IO	20K	8	100	Pd	Tri/0	L
B146	LPTERROR#	I	60K			Tri	Pu	
B147	V_{SS}							
B148	V_{CC}							
B149	ERROR#	I	60K			Tri	Pu	
B150	LPTACK#	I	60K			Tri	Pu	
B151	LPTBUSY	I	20K			Pd	Pd	
B152	LPTPE	I	20K			Pd	Pd	
B153	LPTSLCT	I	20K			Pd	Pd	
B154	LPTD1	IO	20K	8	100	Pd	Tri/0	L
B155	LPTINIT#	OD	4K7	12	100	Tri	Tri	L
B156	LPTD2	IO	20K	8	100	Pd	Tri/0	L
B157	LPTSLCTIN#	OD	4K7	12	100	Tri	Tri	L
B158	LPTD3	IO	20K	8	100	Pd	Tri/0	L
B159	LPTD4	IO	20K	8	100	Pd	Tri/0	L
B160	LPTD5	IO	20K	8	100	Pd	Tri/0	L
B161	LPTD6	IO	20K	8	100	Pd	Tri/0	L
B162	LPTD7	IO	20K	8	100	Pd	Tri/0	L
B163	V_{SS}							
B164	LPTDIR	OD	4K7	12	100	Tri	Tri	L

Table 2-3. 82360SL Pin Characteristics (Continued)

PQFP Pin#	Signal Name	Type	Term	Drive	Load	Susp	ONCE	Derating Curve
B165	V_{CC}							
B166	EXTRTCRW#	O	60K	12	50	Pu	Tri/1	M
B167	EXTRTCDS	O	60K	12	50	Pu	Tri/1	M
B168	EXTRTCAS	O	60K	12	50	Pu	Tri/1	M
B169	RTCRESET#	I	60K			Pu	Pu	
B170	IRQ8	I	60K			Pu	Pu	
B171	IMUX0	I	20K			Pd	Pd	
B172	TIM2CLK2	I	20K			Pd	Pd	
B173	Reserved							
B174	TIM2OUT2	O		12	50	Tri	Tri	M
B175	RTCEN#	I	60K			Pu	Pu	
B176	RTCX2	O					Actv	
B177	RTCVCC							
B178	RTCX1	I					Actv	
B179	V_{SS}							
B180	SMRAMCS#	I	60K			Tri	Pu	
B181	V_{CC}							
B182	SPKR	O		12	50	Tri	Tri	M
B183	HDENH#	O		12	50	Tri	Tri	M
B184	HDENL#	O		12	50	Tri	Tri	M
B185	SUS_STAT#	O		12	50	Drv	Actv	M
B186	EXTSMI#	I	60K			Tri	Pu	
B187	BATTLOW#	I	60K			Pu	Pu	
B188	BATTDEAD#	I	60K			Pu	Pu	
B189	BATTWARN#	I	60K			Tri	Pu	
B190	SRBTN#	I	60K			Pu	Pu	
B191	PWRGOOD	I	60K			Pu	Pu	
B192	IOCS16#	I						
B193	IOCHCK#	I						
B194	DRQ2	I	20K			Pd	Pd	
B195	ONCE#	I	60K			Tri	Pu	
B196	V_{SS}							

3.0 SIGNAL DESCRIPTIONS

386™SL Microprocessor

The following table provides a brief description of the signals of the 386 SL CPU. Signal names which end with the character "#" indicate that the corresponding signal is low when active.

<table>
<tr><th>Symbol</th><th>Name and Function</th></tr>
<tr><td>A20GATE</td><td>A20 Gate: This active HIGH input signal controls the 386 SL CPU A20 address line. When HIGH this signal forces the 386 SL CPU to mask off (force LOW) the internal physical address signal A20. When this signal is LOW, the internal physical address signal A20 is available on the System Address (SA) bus. When A20 gate is inactive this allows emulation of the 8086 1 Mbyte address "wrap-around".</td></tr>
<tr><td>BALE</td><td>Bus Address Latch Enable (ISA bus signal): This active HIGH output signal is used for two purposes. BALE is used to latch the address lines on the LA bus (LA17–LA23) on the falling edge of BALE. BALE is also used to qualify ISA bus cycles for signals on the Peripherial Interface (PI) bus (PM/IO# and PW/R#). On the falling edge of BALE, PM/IO# and PW/R# can be sampled to determine the type of ISA bus cycle that is going to occur. BALE may be used to qualify and generate buffered control and status signals to the ISA expansion bus. The PI bus signal decoding is as follows:
<table>
<tr><th>Type of Bus Cycle</th><th>PM/IO#</th><th>PW/R#</th></tr>
<tr><td>Memory Read</td><td>1</td><td>0</td></tr>
<tr><td>Memory Write</td><td>1</td><td>1</td></tr>
<tr><td>I/O Read</td><td>0</td><td>0</td></tr>
<tr><td>I/O Write</td><td>0</td><td>1</td></tr>
<tr><td>Interrupt Acknowledge</td><td>0</td><td>1</td></tr>
<tr><td>HALT (address = 2)*</td><td>1</td><td>1</td></tr>
<tr><td>Shutdown (address = 0)*</td><td>1</td><td>1</td></tr>
</table>
*Note that BALE is not generated for these cycles, however the PM/IO# and PW/R# will reflect these states during HALT and Shutdown bus cycles where BALE is driven in typical ISA bus systems. Memory read/write, IO read/write and interrupt/interrupt acknowledge cycles correspond to the standard ISA bus cycle.</td></tr>
<tr><td>BUSY#</td><td>BUSY: This active LOW input signal indicates a busy condition from a math co-processor (MCP).</td></tr>
<tr><td>CA[15:1]</td><td>Cache Address Bus: This is the address bus output used to select the memory cell in the cache memory. The CA2 signal is also connected to the CMD0# input of the MCP indicating Opcode (when high) or Data (when low) during a write cycle and control/status register (high) or data register (low) during a read. CA2 is used to address the upper or lower DWORD port of the MCP.</td></tr>
<tr><td>CCSH#</td><td>Cache Chip Select High Byte: This active LOW output is used to enable the upper byte of the cache SRAMs. This signal should be connected to the upper byte cache SRAM chip-select input.</td></tr>
<tr><td>CCSL#</td><td>Cache Chip Select Low Byte: This active LOW output is used to enable the lower byte of the cache SRAMs. This signal should be connected to the lower byte cache SRAM chip-select input.</td></tr>
<tr><td>CD[15:0]</td><td>Cache Data Bus: This is the bi-directional data bus used to transfer data between the cache SRAMs and the 386 SL CPU. The Cache Data bus is also used to transfer data between the MCP and the 386 SL CPU.</td></tr>
</table>

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CMUX0	**CPU Multiplexed Pin Zero:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASL3#" and should be connected to the lower byte of DRAM bank 3 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as an SRAM controller this signal becomes the direction control (DIR) and should be connected to the direction control input of the SRAM data transceiver.
CMUX1	**CPU Multiplexed Pin One:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller then this pin becomes "CASH3#" and should be connected to the upper byte of DRAM bank 3 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this signal becomes "LE" and should be connected to the latch enable input of the SRAM address latch. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX2	**CPU Multiplexed Pin Two:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL2#" and should be connected to the lower byte of DRAM bank 2 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN3#" and should be connected to the data transceiver enable input for bank 3 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX3	**CPU Multiplexed Pin Three:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH2#" and should be connected to the upper byte of DRAM bank 2 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN2#" and should be connected to the data transceiver enable input for bank 2 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not, performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX4	**CPU Multiplexed Pin Four:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL1#" and should be connected to the lower byte of DRAM bank 1 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1#" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX5	**CPU Multiplexed Pin Five:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH1#" and should be connected to the upper byte of DRAM bank 1 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN1#" and should be connected to the data transceiver enable input for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CMUX6	**CPU Multiplexed Pin Six:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASL0#" and should be connected to the lower byte of DRAM bank 0 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN0#" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX7	**CPU Multiplexed Pin Seven:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "CASH0#" and should be connected to the upper byte of DRAM bank 0 CAS# input. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "DEN0#" and should be connected to the data transceiver enable input for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX8	**CPU Multiplexed Pin Eight:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS3#" and should be connected to the upper and lower byte of DRAM bank 3 RAS# inputs. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller then this pin becomes "CE3#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 3 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX9	**CPU Multiplexed Pin Nine:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS2#" and should be connected to the upper and lower byte of DRAM bank 2 RAS# inputs. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE2#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 2 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX10	**CPU Multiplexed Pin Ten:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS1#" and should be connected to the upper and lower byte of DRAM bank 1 RAS# inputs. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE1#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 1 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
CMUX11	**CPU Multiplexed Pin Eleven:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "RAS0#" and should be connected to the upper and lower byte of DRAM bank 0 RAS# inputs. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "CE0#" and should be connected to the upper and lower byte of the SRAM chip-select, or to the chip-select decode logic for bank 0 of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX12	**CPU Multiplexed Pin Twelve:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARL" and should be connected to the lower byte of DRAM bank 0 data parity bit. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OLE#" and should be connected to the lower byte of the SRAM output enable input of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX13	**CPU Multiplexed Pin Thirteen:** This output signal has two functions. When the 386 SL CPU Memory Controller Unit is configured as a DRAM controller this pin becomes "PARH" and should be connected to the upper byte of DRAM bank 0 data parity bit. When the 386 SL CPU Memory Controller Unit is configured as a SRAM controller this pin becomes "OHE#" and should be connected to the upper byte of the SRAM output enable input of the SRAM memory subsystem. This pin is disabled when SUS_STAT# is active (LOW) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
CMUX14	**CPU Multiplexed Pin 14:** This output signal has two functions. The 386 SL CPU can be configured to use this pin as either a BIOS ROM chip-select (ROMCS1#), or a FLASH disk chip-select signal (FLSHDCS#). In either case, the signal is driven LOW when an access to the selected interface occurs.
COE#	**Cache Output Enable:** This active LOW output signal is used to indicate a read access to the CACHE SRAMs, and is used to enable the cache SRAMs' output buffers. This signal should be connected to the output enable signals of the upper and lower byte cache SRAMs.
CPURESET	**CPU Reset:** This active HIGH input forces the 386 SL CPU to execute a reset to the internal CPU core and state machines. The configuration registers are not reset.
CWE#	**Cache Write Enable:** This active LOW output is used to indicate a read (HIGH) or write (LOW) access to the cache SRAMs. This signal should be connected to the write enable signal of the upper and lower cache SRAMs.
DMA8/16#	**DMA 8-bit or 16-bit Cycle:** This input, in conjunction with HRQ, indicates to 386 SL CPU if an 8-bit or 16-bit DMA access is occurring. If an 8-bit DMA access is occurring, the 386 SL CPU will swap the upper byte of data to the lower data byte for upper byte accesses.
EFI	**External Frequency Input.** This is an oscillator input. This clock controls all CPU core and memory controller timings and is equal to twice the desired processor frequency (CLK2 vs CPUCLK).

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
ERROR#	**Numerics ERROR:** This active LOW input to the 386 SL CPU is generated from a math co-processor (MCP). It also indicates to the 82360SL that an unmasked exception has occurred in the MCP. ERROR# is provided to allow numerics error handling compatible with the ISA bus compatible Personal Computer.
HALT#	**HALT:** This active LOW output indicates to external devices that the 386 SL CPU has executed a HALT instruction (address = 2) or a shutdown condition (address = 0). This can be used as an indicator for devices to assert the STPCLK# signal.
HLDA	**HoLD Acknowledge:** This active HIGH output indicates to external devices that the 386 SL CPU has relinquished control of the ISA bus. At this time the 386 SL CPU has floated the address and control signals of the ISA bus.
HRQ	**Hold ReQuest:** This active HIGH input indicates to the 386 SL CPU that an external device wishes to take control of the ISA bus.
INTA#	**INTerrupt Acknowledge:** This active LOW output indicates that the 386 SL CPU is executing an interrupt acknowledge bus cycle. During this process an external interrupt device will pass an interrupt vector to the 386 SL CPU.
INTR	**Interrupt Request:** This active HIGH input indicates to the 386 SL CPU that an external device is requesting the execution of an interrupt service routine.
IOCHRDY	**I/O CHannel ReaDY:** This active HIGH input indicates that the I/O Channel, (ISA expansion bus), is ready to terminate the bus cycle. The ISA expansion bus is a normally ready bus and IOCHRDY is active HIGH. When an ISA bus peripheral needs to extend the standard 3 SYSCLK, 16-bit ISA bus cycle the peripheral device asserts IOCHRDY LOW.
IOCS16#	**I/O Chip Select 16:** This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit I/O cycle. This signal has an active pull-up, when not driven the default I/O bus cycle is 8 bits.
IOR#	**I/O Read:** This active LOW signal indicates that the ISA bus is executing an I/O read cycle.
IOW#	**I/O Write:** This active LOW signal indicates that the ISA bus is executing an I/O write cycle.
ISACLK2	**ISA Clock Two:** This is an oscillator input. This clock controls all of the ISA bus timings and is equal to twice the SYSCLK frequency. Normally the ISA bus SYSCLK is 8 MHz, and the ISACLK2 oscillator is 16 MHz.
LA[23:17]	**Latchable local Address bus:** This is the unlatched local address of the ISA bus for access to memory above 1 megabyte. The LA bus is also used by the Peripherial Interface (PI) Bus.
MA[10:0]	**Memory controller Multiplexed Address bus:** This is the address bus output for the Memory Controller Unit. The 22-bit address is output in a row/column fashion for both DRAM and SRAM memory subsystems. The Memory Controller Unit places the ROW address out first and qualifies it by the RASx# signal going active in DRAM mode or the LE signal going active in the SRAM mode. The column address is then placed on the Memory Address bus and is qualified by the CASXx# signals going active for the DRAM mode. This pin is disabled when SUS_STAT# is active (LOW). When the pin is disabled the output is sustained at the previous state by internal "keepers".

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
MASTER#	**Master:** This active LOW input indicates that an ISA bus peripheral is controlling the bus. The peripheral device asserts this signal in conjunction with a DMA request (DRQ) line or the HRQ (hold request) to gain control of the bus. When the MASTER# signal is asserted LOW along with HRQ being asserted HIGH or a DRQ line being asserted HIGH, the 386 SL CPU will float all address, data and control signals on the ISA bus.
MD[15:0]	**Memory controller local Memory Data bus:** This is the bi-directional data bus of the Memory Controller Unit. All accesses by the Memory Controller Unit that transfer data between the 386 SL CPU and SRAM or DRAM use the Memory Data Bus. This pin is disabled when SUS_STAT# is active (low) and the system is not performing a suspend refresh operation. When the pin is disabled the output is sustained at the previous state by internal "keepers".
MEMCS16#	**MEMory Chip Select 16:** This active LOW input indicates that an ISA bus peripheral wishes to execute a 16-bit memory cycle. This signal has an active pull-up, when not driven the default memory bus cycle is 8 bits.
MEMR#	**MEMory Read:** This bi-directional active LOW signal indicates when a memory read access is taking place on the ISA bus. When the 386 SL CPU is performing a memory read to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA device or Master drives MEMR#.
MEMW#	**MEMory Write:** This bi-directional active LOW signal indicates when a memory write access is taking place on the ISA bus. When the 386 SL CPU is performing a memory write to the ISA bus it is an output, when the DMA or Bus Master is accessing memory on the ISA bus, the DMA controller or Bus Master drives MEMW#.
N/C	**No connection:** These pins must not be connected to any voltage, but must be left floating in order to guarantee proper operation of the 386 SL CPU and to maintain compatibility with future Intel Processors.
NMI	**Non-Maskable Interrupt:** This rising edge sensitive input will latch a request to the 386 SL CPU for a non-maskable interrupt on a LOW-to-HIGH transition.
NPXADS#	**Numerics ADdress Strobe:** This active LOW output signal indicates the start of a math co-process (MCP or NPX, numerics processor extension) data transfer cycle.
NPXCLK	**Numerics Clock:** This output signal is used to drive the MCP clock input.
NPXRDY#	**Numerics Ready:** This active LOW input is used to terminate a MCP (or NPX, numerics processor extension) bus cycle. This signal is low for I/O and data operand MCP cycles.
NPXRESET	**Numerics Reset:** This active HIGH output signal is used to reset the MCP.
NPXW/R#	**Numerics Write or Read:** This output signal indicates the type of data transfer that is being performed between the 386 SL CPU and the MCP. When high this signal indicates a MCP write, when low this signal indicates a MCP read.
ONCE#	**ON-board Circuit Emulation:** This active LOW input signal floats the neccessary outputs from the 386 SL CPU allowing an in-circuit emulation (ICE™-386™SL) module to drive the 386 SL CPU signals. This allows an emulator to be used for system testing and developement while the 386 SL CPU and the 82360SL are still physically populated on the system motherboard. The state of all 386 SL CPU and 82360SL signals when ONCE# is asserted low is summarized in section 2, (386 SL CPU and 82360SL signal characteristics).

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
PCMD#	**PI-BUS Command:** This active LOW output indicates that valid write data is on the System data bus (SD[15:0]) signals, or that the 386 SL CPU is ready to sample valid read data from the PI bus for Peripherial Interface bus cycles.
PEREQ	**Processor Extension Request:** This active HIGH output signal indicates that the 386 SL CPU has data to transfer to or from the MCP data FIFO.
PERR#	**Parity ERRor:** This active LOW output indicates to an external device that the 386 SL CPU Memory Controller Unit has detected a memory parity error. The PERROR# signal is used by the 82360SL to generate NMI back to the 386 SL CPU.
PM/IO#	**PI-BUS Memory or I/O:** This output indicates the type of bus cycle the 386 SL CPU is executing on the Peripherial Interface Bus (PI-bus): Either a Memory (HIGH) or I/O (LOW) cycle.
PRDY#	**PI-BUS Ready:** This active LOW input is used to terminate Peripherial Interface bus cycles. The Peripheral Interface Bus is a normally not-ready bus, and will continue the bus cycle until the PRDY# is activated or a Peripherial Interface Time-out occurs.
PSTART#	**PI-BUS START:** This active LOW output indicates that the address (SA[19:0], LA[23:17] and SBHE#), command signals (PM/IO# and PW/R#) and chip-selects (VGACS# or FLSHDCS#) are valid for a Peripheral Interface Bus cycle.
PW/R#	**PI-BUS Write or Read:** This output indicates the type of bus cycle the 386 SL CPU is executing on the Peripheral Interface Bus: Either a Write (HIGH) or Read (LOW) cycle.
PWRGOOD	**Power Good:** This active HIGH input indicates that power to the system is good. This signal is generated by the power supply circuitry, and a LOW level on this signal causes the 386 SL to totally reset: The CPU core is reset, internal state machines are reset, all configuration registers are reset. Power Good should be low for a specified minimum number of CPU clocks for valid recognition in order to perform a global 386 SL CPU reset.
REFREQ	**REFresh REQuest:** This active HIGH input indicates that the 386 SL CPU should execute an internal DRAM refresh cycle to the on-board local memory.
ROM16/8#	**ROM 16-bits or 8-bits:** This input configuration signal pin selects if the BIOS interface is a 16-bit (when high) or 8-bit interface (when low). This pin has an internal pull-up resistor defaulting to a 16-bit wide BIOS EPROM.
ROMCS0#	**ROM Chip Select 0:** This LOW true output provides the chip select for the System BIOS EPROM.
SA[19:0]	**System Address Bus:** This is the bi-directional system address of the ISA bus, as well as the Peripheral Interface Bus. SA[16:0] are inputs during DMA and Master operation. SA[19:17] are outputs only since a 8237 compatible DMA controller accesses up to 64 kBytes at a time. The 74LS612 module in the 82360SL is used to furnish the DMA upper addresses for DMA access to 16 Megabyte.
SBHE#	**System Byte High Enable:** When this output signal is LOW, it indicates that data is being transferred on the upper byte of the 16-bit data bus (SD[15:8]).
SD[15:0]	**System Data Bus:** This 16-bit bi-directional data bus is used to transfer data between the 386 SL CPU and the ISA bus. The system data bus is also used to transfer data between the 386 SL CPU and the Peripherial Interface (PI-BUS).
SMI#	**System power Management Interrupt:** This falling edge sensitive input latches a Power Management interrupt request with a High-to-Low edge. The SMI# is the highest priority interrupt in the 386 SL processor.

386™SL Microprocessor Signal Descriptions (Continued)

Symbol	Name and Function
SMRAMCS#	**System power Management RAM Chip Select:** This active LOW output is used to select an external system power management SM-RAM, and to indicate to the 82360SL device when accesses to the system power management SM-RAM are occurring.
STPCLK#	**Stop Clock:** This active LOW input stops the clock to the internal 386 CPU core. (This signal is functionally tested by the execution of HALT or I/O read instructions.)
SYSCLK	**System Clock:** This is a clock output equal to one half of the ISACLK2 input frequency.
SUS_STAT#	**SUSpend STATus:** This active LOW input indicates to the 386 SL CPU that system power is being turned off. The 386 SL CPU will respond by electrically isolating selected pins as indicated in Section 2, (386 SL CPU signal characteristics).
TURBO	**Turbo:** This active HIGH input signal indicates to 386 SL CPU when to enter "Turbo Mode". Turbo Mode is defined as the CPU executing at full speed, the default speed for the system. When this signal is forced inactive LOW, the 386 SL CPU executes from a divide by two or a divide by four clock as defined by the De-turbo bit in the CPUPWRMODE register. When this signal is HIGH, the CPU executes from a clock as defined by the Fast CPU clock field in the CPUPWRMODE register.
V_{CC}	**System Power:** Provides the +5V nominal D.C. supply inputs.
VGACS#	**VGA Chip-select:** This active LOW output is asserted anytime an access occurs to the user defined VGA address space.
V_{SS}	**System Ground:** Provides the 0V connection from which all inputs and outputs are referenced.
WHE#	**Write High Enable:** This active LOW output indicates that a write access to the upper byte of the 386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the upper byte for either DRAM or SRAM memory subsystems. This pin is driven during a suspend operation.
WLE#	**Write Low Enable:** This active LOW output indicates that a write access to the lower byte of the 386 SL CPU memory bus is occurring when the Memory Controller Unit is configured for SRAM mode. When in DRAM mode, the signal is active anytime a write access occurs. This output should be connected to the write enable of the lower byte for either DRAM or SRAM memory subsystems. This pin is driven during a suspend operation.
ZEROWS#	**ZERO Wait State (ISA bus signal):** This active LOW input indicates that an ISA bus peripheral wishes to execute a zero wait state bus cycle (the normal default 16-bit ISA bus memory or I/O cycle is 3 SYSCLKs or one PC/AT equivalent wait state). When ZEROWS# is driven low, a 16-bit bus cycle will occur in two SYSCLKs. When ZEROWS# is driven low for an 8-bit memory cycle the default 6 SYSCLK bus cycle is shortened to 3 SYSCLKs.

3.0 SIGNAL DESCRIPTIONS (Continued)

82360SL ISA Peripheral I/O

The following table provides a brief description of the signals of the 82360SL I/O. Signal names which end with the character "#" indicate that the corresponding signal is low true when active.

Symbol	Name and Function
A20GATE	**A20 Gate (direct to CPU):** This active HIGH output signal forces the 386 SL CPU to mask off A20 on the system address bus (internal to the 386 SL CPU), to allow emulation of an 8086.
AEN	**Address ENabled (ISA-bus signal):** This active HIGH output indicates a DMA access, refresh or I/O access to a non-standard ISA peripheral I/O address location. The 82360SL drives this signal high to signify a valid DMA address. It is used by bus slaves to decode I/O ports. All ports must be decoded for AEN low. There are no DMA cycles to addressed I/O ports.
BALE	**Buffered Address Latch Enable (ISA-bus signal):** This active HIGH input to the 82360SL is driven by the 386 SL CPU during standard ISA bus cycles. During ISA bus memory and I/O cycles BALE is used to indicate valid addresses at the start of a bus cycle. SA[19:0] are valid on the falling edge and LA[23:17] are valid while BALE is high. BALE is is also driven high by the 386 SL CPU and remains high during DMA cycles.
BATTDEAD#	**BATTery DEAD:** This active LOW input indicates that the battery does not have enough power to resume or reset. This signal will prevent a system reset if asserted LOW.
BATTLOW#	**BATTery LOW:** This active LOW input indicates that the battery power is low. BATTLOW# is typically driven by a D.C. to D.C. power converter associated with the battery power supply. A thermal power monitor indicates that the main battery power is dropping below the adequate charge level to sustain operation. If this signal is asserted LOW with BATTWRN# asserted LOW a SMI request will be generated. The feature is enabled via S/W control. The signal will also prevent a resume operation if asserted LOW.
BATTWARN#	**BATTery WARNing:** This active LOW input indicates the battery has minimal charge left (eg. one half an hour of full power use remaining).
C8042CS#	**Keyboard controller Chip Select:** This active LOW output is driven when there is an I/O read or write to the Keyboard Controller Ports 60 or 64 hex.
COM(A,B)CTS#	**Clear To Send:** This active LOW input indicates to the Serial Port Controller for COMA or COMB that a serial device is clear to accept data. This signal is typically used for a modem control function. A change in the state of this signal generates a modem status interrupt. The modem or data set asserts this signal when it is ready to accept data for transmission.
COM(A,B)DCD#	**Data Carrier Detect:** This active HIGH input indicates that the Serial Port Controller COMA or COMB has detected a data carrier from the data set of a serial device. Typically this signal is from a modem.
COM(A,B)DSR#	**Data Set Ready:** This active LOW input signal is used by the modem or data set to indicate that the modem or data set is ready to establish the communication link and transfer data with the Serial Port Controller.
COM(A,B)DTR#	**Data Terminal Ready:** This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to communicate.
COM(A,B)RXD	**Serial data Receive:** This input signal is used to receive serial data. Each character can consist of from five to eight bits of data with one start bit and one, one and a half or two stop bits. The least significant bit is received first.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
COM(A,B)RI#	**Ring Indicator:** This active LOW input signal is used for a modem control function. A change in the state (either from high to low or from low to high) of this signal generates a modem status interrupt. The modem or data set asserts this signal to indicate that it has detected a telephone ring. This will cause the 82360SL to wake the 386 SL CPU from a suspended state if modem ring is enabled as a wake-up event.
COM(A,B)RTS#	**Request To Send:** This active LOW output signal informs the modem or data set that the Serial Port Controller is ready to send data.
COM(A,B)TXD	**Serial data transmission:** This output signal is used to transmit data serially between the Serial Port Controller and serial device. Each character can consist of five to eight bits of data with one start bit and either one, one and a half, or two stop bits. The least significant bit is transmitted first. The control of the format of a character is defined under S/W control via the Line Control Register. Please consult the 386 SL Microprocessor SuperSet Programmer's Reference Manual for additional information. Information regarding the functional timing specifications of transmitted and recieved serial data may be found in sections 6 and 7 (A.C. timing specifications and timing diagrams).
COMX1,COMX2	**Crystal oscillator input and output pins:** The crystal attached to these signals should be tuned to 1.8432 Mhz. The on-chip oscillator uses an external crystal and tank circuit to generate an internal clock. This clock is used to generate the various baud rates for the serial ports. Optionally an external oscillator may be connected to the COMX1 input.
CPURESET	**CPU RESET:** This active HIGH output is connected directly to the 386 SL CPU to provide a reset of the 386 CPU core. CPURESET always occurs during a PWRGOOD reset. CPURESET may also be generated by RC# from a keyboard controller, Fast Reset from I/O Port 92 or other programmable Reset, or a resume from suspend.
CX1,CX2	**Crystal oscillator input and output pins:** The crystal should be tuned to 14.31818 Mhz. It is used for the ISA bus signal OSC signal and is internally divided by 12 to clock the timer counters. The oscillator input may be directly driven from an external source.
DACK[7:5], [3:0]#	**DMA ACKnowledge channel n (ISA bus signal):** The 82360SL DMA controller drives the respective DMA acknowledge signal low after a device has requested DMA service. The corresponding output signal indicates that the DMA channel transfer may begin.
DMA8/16#	**DMA 8-bit or 16-bit cycle:** This output signal is directly connected to the 386 SL CPU. When the signal is HIGH it indicates that the current DMA cycle is 8-bit. When this signal is low it indicates that the DMA cycle is using a 16-bit channel.
DRQ[7:5], [3:0]	**DMA ReQuest channel n (ISA bus signal):** These input signals are used to request DMA service from devices residing on the ISA bus. An ISA bus device drives this signal to request service from the appropriate DMA channel by asserting this signal high.
ERROR#	**MCP ERROR:** This signal is an active LOW input to the 82360SL. The math coprocessor error signal generates a IRQ13 through the 82360SL.
EXTSMI#	**EXTernal System Management Interrupt request:** This active low input will generate a SMI request if the function is enabled.
EXTRTCAS	**EXTernal RTC Address Strobe:** This output signal is active HIGH when there is a write access to the RTC I/O address port and when an external RTC is selected.
EXTRTCDS	**EXTernal RTC read Data Strobe:** This output signal is active LOW when there is a read access to an external RTC I/O data port and when an external RTC is selected.
EXTRTCRW#	**EXTernal RTC (Real Time Clock) Read/Write:** This low true output signal is active when there is a write access to an external RTC I/O data port and when an external RTC is selected.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
FLPCS#	**FLoPpy Chip Select:** This LOW true output signal is the chip select for the floppy disk controller I/O ports 03F0–03F5 and 3F7 hex.
HALT#	**HALT:** This LOW true input signal is driven by the 386 SL CPU and indicates when the CPU has executed a HLT instruction (address = 2) or is in a shutdown condition (address = 0).
HD7	**HD-bus Data bit HD7:** The bi-directional System Data Bit 7 is controlled separately for the Integrated Drive Electronics (I.D.E.) hard disk drive and floppy disk drive. This is provided to accommodate the I/O address 3F7 hex which is split between the floppy disk drive controller and I.D.E. hard disk. Data transfer between storage peripherals connected to the I.D.E. Hard Disk and Floppy Disk and the 82360SL are on separate busses. Data bit 7 has to be separated from data bits [6:0]. The 82360SL controls and buffers data bit 7 seperately.
HDCS[1:0]#	**Hard Disk Chip Select:** These LOW true output signals are the I.D.E. hard disk drive chip selects decoded from the I/O address ports 01F0–01F7h (HDCS0#) and 03F6–03F7h (HDCS1#).
HDEN(H,L)#	**Hard Disk buffer ENable:** These LOW true output signals control the I.D.E. hard disk data buffers, high and low bytes.
HLDA	**HoLD Acknowledge (direct to CPU):** This HIGH true input signal indicates that the 386 SL CPU has released the ISA bus for refresh, DMA or master cycles.
HRQ	**Hold ReQuest (direct to CPU):** This active HIGH output signal indicates a request to the 386 SL CPU to release the ISA bus when the 82360SL requests the bus for ISA bus style refresh, DMA or master mode cycles.
IMUX0	This pin is multiplexed. It can be used as Timer 2 gate 2 input or a speaker input from the modem.
INTA#	**INTerrupt Acknowledge (direct to CPU):** This active LOW input to the 82360SL indicates that the 386 SL CPU has recognized an interrupt and will initiate an interrupt acknowledge bus cycle. The INTA bus cycle is comprised of two eight-bit I/O cycles in which the interrupt vector transferred on the second eight-bit I/O write of the INTA cycle.
INTR	**INTerrupt Request (direct to CPU):** This active HIGH output requests a standard maskable interrupt to the 386 SL CPU.
IOCHCK#	**IO CHannel CheckK (ISA bus signal):** This maskable active LOW input is driven by a device on the ISA bus typically used to indicate a parity error on the ISA bus. This signal is one of the possible sources which may generate an NMI. NMI generation via IO Channel Check may be enabled or disabled using PORT 61 (IOCKEN). NMI may be masked using the ISA bus compatible NMI control port at I/O 70 hex bit 7.
IOCHRDY	**I/O CHannel ReaDY (ISA bus signal):** This active HIGH input is used by the 82360SL DMA controller to extend ISA bus cycles. IOCHRDY is also used to extend bus cycles for I/O device trapping. Additional wait states extend the bus cycle, allowing for start up during Resume mode. The ISA bus is a normally ready bus, an external device can extend a DMA cycle or ISA bus cycle by deasserting this signal (driven low). This signal is normally high on the ISA bus.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
IOCS16#	**16-bit I/O Chip Select (ISA bus signal):** This active LOW input signal to the 82360SL is used to indicate a 16-bit I/O bus cycle. The I.D.E. hard disk high byte buffer enable is generated when IOCS16# is driven low during an I.D.E. 16-bit I/O access. IOCS16# is also an input to the 386 SL CPU driven by devices residing on the ISA bus to indicate a 16-bit I/O bus cycle.
IOR#	**I/O Read (ISA bus signal):** This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates an I/O read. This signal is an output from the 82360SL during DMA bus cycles for I/O to memory transfers.
IOW#	**I/O Write (ISA bus signal):** This bi-directional active LOW signal is an input during normal accesses to I/O ports. When low this signal indicates and I/O write. This signal is an output from the 82360SL during DMA bus cycles for memory to I/O transfers.
IRQ[15, 14, 12-3, 1]	**Interrupt ReQuest n (ISA bus signal):** These active HIGH input signals are used to request interrupt service. The interrupt request lines are driven by devices on the ISA bus which have a corresponding interrupt service routine associated with the interrupt vector and interrupt request.
KBDA20	**KeyBoarD A20 gate:** This active HIGH input is "ORed" with internal bits to produce A20GATE which goes to the 386 SL CPU. The bit is connected to port 2, bit 1 of an 8042 in a standard ISA bus compatible system.
KBDCLK	**KeyBoarD CLocK:** This output signal is used to drive the clock input to the keyboard controller. It is derived from the 8 MHz SYSCLK and can be divided by 1, 2, 4 or stopped.
LA[23:17]	**Local Address bus (ISA bus signal):** These are input signals to the 82360SL during memory transfers (decoding for X-bus buffer controls) and output signals during DMA accesses and refresh. The latchable address lines allow access to physical memory on the ISA bus to 16 megabytes.
LPTACK#	**Line PrinTer ACKnowledge:** Active LOW input signal which is part of the parallel port data handshake. The line printer asserts this signal to show that data transfer was complete and that it is ready for the next transfer.
LPTAFD#	**Line Printer Auto line FeeD:** This signal is an active LOW output from 82360SL to a printer. When asserted, it instructs the printing device to insert a line feed at the end of every line.
LPTBUSY	**Line PrinTer BUSY:** This signal is an active HIGH input to 82360SL. The printer asserts this signal when it is not ready to accept further data from 82360SL.
LPTD[7:0]	**Line printer Data bus:** These signals are the 8-bit bi-directional data bus for the parallel port. In PC/AT mode these signals are output only. The 82360SL also supports a bidirectional mode for the PS/2 style parallel port.
LPTDIR	**Line PrinTer DIRection:** This active HIGH output signal is only valid in bidirectional mode for data transfer using the parallel port.
LPTERROR#	**Line PrinTer ERROR:** This active LOW input signal is driven by a peripheral device to flag an error condition.
LPTINIT#	**Line PrinTer InITialize:** This active LOW output from 82360SL instructs the peripheral to initialize itself.
LPTPE	**Line PrinTer Paper End:** This active HIGH input to 82360SL signals that the printer has run out of paper when asserted.
LPTSLCT	**Line PrinTer SeLeCTed:** This active HIGH input signal is asserted by the printer to confirm that it has been selected.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
LPTSLCTIN#	**Line PrinTer SeLeCT IN:** This active LOW output signal is asserted to select the printer interfaced to the parallel port.
LPTSTROBE#	**Line PrinTer STROBE:** This active LOW output signal is used to strobe data into the peripheral device. The parallel port controls are read and written through I/O registers.
MASTER#	**ISA bus MASTER (ISA bus signal):** This active LOW input signal is used with a DRQ line to gain control of the system bus. Upon receiving DACK# the 82360SL may pull MASTER# active (low), which will allow the 82360SL control of the system address, data and control busses. The 386 SL CPU will have tri-stated these lines one clock after receiving the MASTER# signal.
MEMR#	**MEMory cycle Read (ISA bus signal):** This bi-directional active LOW signal indicates a read cycle anywhere in the 16 Mbyte memory address space. During memory read cycles to memory on the ISA bus, this signal is an input into the 82360SL. MEMR# is driven by the 82360SL during DMA cycles.
MEMW#	**MEMory cycle Write (ISA bus signal):** This bi-directional active LOW signal indicates a write cycle anywhere in the 16 Mbyte memory address space. During memory write cycles to memory on the ISA bus, this signal is an input. MEMW# is an output from the 82360SL during DMA cycles.
N/C	**No Connection:** These signals must not be connected to any voltage. The No Connection signals must be left floating in order to guarantee proper operation of the 82360SL and compatibility with future Intel processors.
NMI	**Non Maskable Interrupt (direct to CPU):** This active HIGH output is directly connected to the 386 SL CPU. The 82360SL asserts NMI to request the 386 SL CPU to service a high priority non-maskable interrupt. The low to high transition of this signal is recognized by the 386 SL CPU.
ONCE#	**ON-board Circuit Emulation:** This active LOW input pin floats the appropriate outputs of the 82360SL as indicated in Section 2 pin assignments. When ONCE# is driven active the 82360SL allows an In-Circuit emulator (ICE™-386™SL) module to drive its signals. This allows the system to be tested while the 82360SL is still physically populated on the motherboard.
OSC	**OSCillator (ISA bus signal):** This is the 14.31818 Mhz output signal with a 50% duty cycle and is asynchronous to SYSCLK.
PERR#	**Parity ERRor (direct from CPU):** This active LOW input signal is connected to the output of the 386 SL CPU. When the 386 SL CPU detects a parity error from the local DRAM subsystem it drives this signal to the 82360SL. The system memory parity error will generate a NMI via the 82360SL when NMI is enabled via I/O port 70 hex bit 7.
SMI#	**System Management Interrupt (direct to CPU):** This active LOW output is directly connected to the 386 SL CPU. When the falling edge of SMI# is detected by the 386 SL CPU it generates the highest priority interrupt when enabled. The typical use of SMI# is for power management.
SMRAMCS#	**System Management RAM Chip Select:** This active LOW output is driven whenever the 386 SL CPU is accessing the System Management SM-RAM. It is active even when SM-RAM is part of the 386 SL CPU system memory RAM. The 82360SL uses the SMRAMCS# to determine when the SMI code is being executed on the ISA bus, and enables the X-bus control signals.
PWRGOOD	**PoWeR GOOD:** This active HIGH input is typically supplied by the power supply. When Power good is activated high this indicates that the supply voltage is stable. Power Good low is also used to generate System Reset, RESETDRV, and CPURESET.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
RC#	**Reset CPU:** This active low input is typically driven by the keyboard controller. RC# is "ORed" with internal bits to produce a programmable pulse width CPURESET signal. It is connected to port 2, bit 0 of an 8042 in a standard ISA bus compatible system.
REFREQ	**REFresh REQuest (direct to CPU):** This active HIGH output signal is directly connected to the 386 SL CPU. When Refresh Request is asserted it indicates that the 386 SL CPU should refresh the local DRAM subsystem.
REFRESH#	**System REFRESH (ISA bus signal):** This active LOW input signal indicates a refresh cycle. It is driven for the duration of the cycle. It is an input during master generated refresh bus cycles.
RESETDRV	**RESET DRiVe (ISA bus signal):** This active HIGH output is the main system cold reset, generated from the power supply "power good" signal and by system resume.
RTCEN#	**RTC ENable:** This active LOW input signal should be strapped high or low depending on whether an internal (LOW) or external (HIGH) RTC is used in the system. The 82360SL on-chip real time clock and CMOS RAM are enabled by this signal when LOW.
RTCRESET#	**Internal RTC RESET input:** This active LOW input signal is used to reset the internal RTC status and flag registers, (typically when the RTC battery has been changed).
RTCVCC	This is a separate power supply input for the internal RTC. It should be connected to a 3V battery when the system is fully off and 5V during active operation.
RTCX1,RTCX2	**RTC Crystal oscillator input and output pins:** The crystal should be tuned to 32.768 Khz. It is used for the RTC and system power management state machines. The oscillator may be driven directly from the input signal.
SA[16:0]	**System Address bus (ISA bus signal):** The bi-directional system address bus is an input for decoding internal I/O registers and an output during DMA and refresh cycles.
SBHE#	**System Byte High Enable (ISA bus signal):** The active LOW output signal indicates when there is valid data on the upper data byte of the system data bus.
SD[7:0]	**System Data bus (ISA bus signal):** This is the bidirectional system data bus. The 82360SL directly drives the ISA bus system data bits [7:0] without external transceivers or buffers. 8-bit data is transferred to and from the 82360SL with these signals.
SMEMR#	**System MEMory Read (ISA bus signal):** This signal is driven by the 82360SL to signify a memory read cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles.
SMEMW#	**System MEMory Write (ISA bus signal):** This signal is driven by the 82360SL to signify memory write cycle to the bottom 1 Mbyte address range. It is used by ISA bus compatible slaves which decode SA[19:0] during memory cycles.
SMOUT[5:0]	**System Management OUTput control:** These six outputs can be connected to control the power circuits for various devices in the system. These output pins are directly controlled by the SM_OFF_CNTRL register.
SPKR	**SPeaKeR output:** This is the output of the 8254 megacell, timer/counter #1, channel 2, or directly driven through IMUX0, or from the 8254 megacell, timer counter #2, channel 1. This output signal is typically connected to an external speaker. There is additional circuitry to ensure that the signal is low when not being used.
SRBTN#	**Suspend/Resume BuTtoN:** This active LOW input generates a SMI requesting a system suspend or resume.

82360SL ISA Peripheral I/O Signal Descriptions (Continued)

Symbol	Name and Function
STPCLK#	**SToP CLocK:** This active LOW output signal stops the clock to the 386 CPU core of the 386 SL Microprocessor. Stop clock is directly connected to the 386 SL CPU from the 82360SL. The 82360SL activates this signal upon detection of a halt bus cycle or when an I/O read to the stop clock register in the 82360SL occurs.
SYSCLK	**SYStem CLocK (ISA bus signal):** This signal is an output from the 386 SL CPU and an input to the 82360SL. The SYSCLK signal is used to clock the ISA bus state machines and is also used to derive the internal DMA clock signal in the 82360SL. The SYSCLK is the 8 MHz typical clock which is one half of the frequency of ISACLK2.
SUS_STAT#	**SUSpend STATus:** The 82360SL power management controls this active low output signal to switch the power off to all non-critical devices during a suspend.
TC	**Terminal Count (ISA bus signal):** This active HIGH output signal is used to indicate the termination of a DMA transfer.
TIM2CLK2	**TIMer 2 CLK:** This is the input clock for timer/counter #2 when it is programmed to be used in the General Purpose (GP) mode.
TIM2OUT2	**TIMer 2 OUTput:** This signal is the frequency output from timer/counter #2 and can be used as a general purpose timer/counter output.
V_{CC}	**System Power:** Provides the + 5V nominal D.C. supply inputs for the 82360SL.
V_{SS}	**System Ground:** Provides the 0V connection from which all inputs and outputs are referenced.
XD7	**X-bus Data bit XD7:** I/O port 3F7h is split between the floppy and hard disk and the storage peripherals which transfer data reside on separate busses. Data bit XD7 is separated from bits XD[6:0]. The 82360SL separately controls and buffers bit XD7 to isolate data bit 7 from the floppy disk and I.D.E. hard disk.
XDEN#	**X-bus Data ENable:** This active LOW output signal is used to control the X-bus data transceiver. It is only activated by the 82360SL on valid accesses to X-bus peripherals.
XDIR	**X-bus data DIRection:** This active HIGH output signal controls the direction of the X-bus and HD-bus data transceivers. XDIR is high for read cycles.
ZEROWS#	**ZERO Wait State (ISA-bus signal):** This active LOW output signal is driven by the 82360SL when it can accept a zero wait state write cycle.

4.0 PACKAGE THERMAL SPECIFICATIONS

The SL SuperSet is specified for functional operation with a temperature range from 0 to 90 degrees Celcius for the 386 SL CPU and the 82360SL. The case temperature should be measured in the operating environment to determine whether the SL SuperSet is within the specified operating temperature range. The case temperature should be measured at the center of the top surface of the package. When the SL SuperSet devices have a supply voltage applied the operating temperature range is applicable rather than the storage temperature.

The following definitions and assumptions are used to determine the recommended maximum case temperature for the 386 SL CPU and 82360SL:

T_A = Ambient Temperature in degrees Celcius

T_C = Case temperature in degrees Celcius

θ_{JC} = Package thermal resistance between junction and case

θ_{JA} = Package thermal resistance between junction and ambient

T_J = Junction Temperature

P = Power Consumption in Watts

The ambient temperature can be evaluated by using the values of thermal resistance between junction and case, θ_{JC} and the thermal resistance between junction and ambient θ_{JA} in the following equations:

$$T_J = T_C + P*\theta_{JC}$$

$$T_A = T_J - P*\theta_{JA}$$

$$T_C = T_A + P*[\theta_{JA} - \theta_{JC}]$$

Values for θ_{JA} and θ_{JC} are given in Table 4-1 for the 196-lead PQFP 82360SL and the 227-lead LGA 386™SL CPU.

Table 4-1. Thermal Resistances (°C/W) θ_{JC} and θ_{JA}

Package	θ_{JC} °C/W	θ_{JA} (°C/W) versus Airflow—ft/min (m/sec)					
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
196L PQFP	5	21	18	13.5	11.8	10.5	9.5
227L LGA							

ABSOLUTE MAXIMUM RATINGS

Table 4.3 provides environmental stress ratings for the packaged SL SuperSet devices. Functional operation at the storage maximum and minimum ratings is not implied or guaranteed.

Extended exposure to maximum ratings may affect device reliability. Further, precautions should be taken to avoid high static voltages and electric fields to prevent static electric discharge.

Other system components such as the memory subsystem (DRAM/SRAM), storage peripherals (hard disk/floppy disk), I/O and display subsystem may reduce the absolute maximum storage temperature conditions due to the inherent physical characteristics of the other components.

Table 4-3. Maximum Ratings

Parameter	Maximum Rating
1. Storage Temperature	−65°C to +150°C
2. Case Temperature under Bias	0°C to +90°C(1)
3. Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V
4. Voltage on Other Pins	−0.5V to (V_{CC} + 0.5V)

NOTE:
1. Case temperature under Bias maximum rating also includes the case where the 386 SL CPU and 82360SL are in suspend or standby mode. In standby mode and in specific cases in suspend mode, power is applied to the SL SuperSet for operation of the Real-Time Clock and DRAM refresh. It is assumed in these cases that the SL SuperSet devices are not in normal or full-speed operation. Typically at these extreme minimum and maximum temperature ranges the external oscillators are stopped or diasbled with the exception of the 32 kHz Real-Time Clock oscillator. The limiting factor for minimum and maximum case temperature under Bias is the operational temperature range supported by the RTC crystal and 82360SL on-chip oscillator. It is also assumed that main system memory is not being accessed (only slow refresh for DRAM) or the SRAM is in standby mode, and all other components used in the system are also capable of operating at these maximum and minimum temperature values.

5.0 D.C. SPECIFICATIONS

386™SL CPU D.C. Specifications

Functional operating range: V_{CC} = 5V ± 10%; T_{CASE} = 0°C to 90°C

Table 5-1. D.C. Voltage Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Inpt Low Voltage	−0.3	0.8	V	At 8 MHz
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	At 8 MHz
V_{ILC}	EFI/ISACLK2 Input Low Voltage	−0.3	0.8	V	At 8 MHz, CMOS Logic Levels
V_{IHC}	EFI/ISACLK2 Input High Voltage	V_{CC} − 0.8	V_{CC} − 0.3	V	At 8 MHz, CMOS Logic Levels
V_{OL}	Output Low Voltage				
	I_{OL} = 4 mA		0.5	V	At 8 MHz(1)
	I_{OL} = 24 mA		0.5	V	At 8 MHz(2)
V_{OH}	Output High Voltage				
	I_{OH} = −2 mA	2.4		V	At 8 MHz(1)
	I_{OH} = −0.2 mA	V_{CC} − 0.5		V	At 8 MHz(2)
	I_{OH} = −4 mA	2.4		V	At 8 MHz(2)
	I_{OH} = −0.18 mA	V_{CC} − 0.5		V	At 8 MHz(1)

Table 5-2. Leakage Current and Sustaining Current Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{IL}	Input Leakage Current Condition 1: When SUS_STAT# and/or ONCE# not active. Pins with internal 60k PU Pins with internal 20k PD Pins with internal 300 PU Other Input Pins		 −150 300 −24 ±15	 μA μA mA μA	 V_{IL} = 0.45V V_{IH} = 2.4V V_{IL} = 0.45V 0V < V_{IN} < V_{CC}
	Condition 2: When SUS_STAT# and/or ONCE# active. Pins with internal 60k PU Pins with internal 20k PD Pins with internal 300 PU Other Input Pins		 ±15 ±15 ±15 ±15	 μA μA μA μA	 0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC} 0V < V_{IN} < V_{CC}
I_{OL}	Output Leakage Current Condition 1: When SUS_STAT# and/or ONCE# not active Pins with internal 60k PU Pins with internal 300 PU Other Output Pins		 −60 −24 ±15	 μA mA μA	 V_{OUT} = 0.45V V_{OUT} = 0.45V 0.45V < V_{OUT} < V_{CC}
	Condition 2: When SUS_STAT# and/or ONCE# active Pins with internal 60k PU Pins with internal 300 PU Other Output Pins		 ±15 ±15 ±15	 μA μA μA	 0.45V < V_{OUT} < V_{CC} 0.45V < V_{OUT} < V_{CC} 0.45V < V_{OUT} < V_{CC}
I_{BHL}	Input Sustaining Current (Bus Hold Low)		38	μA	V_{IN} ≤ 0.8V(3,4)
I_{BHH}	Input Sustaining Current (Bus Hold High)		−60	μA	V_{IN} ≥ 3.0V(3,5)
I_{BHLO}	Bus Hold Low Overdrive		300	μA	(Notes 3, 6)
I_{BHHO}	Bus Hold High Overdrive		−550	μA	(Notes 3, 7)

Table 5-3. Capacitance D.C. Specifications

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		10	pF	EFI = 1 MHz(8)
C_{OUT}	Output or I/O Capacitance		20	pF	EFI = 1 MHz(8)
C_{CLK}	EFI Capacitance		15	pF	EFI = 1 MHz(8)

NOTES:
1. List of pins which have 24 mA/4 mA I_{OL}/I_{OH} specification, (reference section 2).
2. Other output pins which do not belong to list in Note 1, (reference Section 2).
3. Tested with CPU Clock stopped.
4. This is the maximum current the bus hold circuit can sink without raising the node above 0.8V. I_{BHL} should be measured after lowering V_{IN} to Ground (0V) and then raising to 0.8V.
5. This is the maximum current the bus hold circuit can source without lowering the node voltage below 3.0V. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering to 3.0V.
6. An external driver must source at least I_{BHLO} to switch this node from low to high.
7. An external driver must sink at least I_{BHHO} to switch this node from high to low.
8. Not tested. Guaranteed by design characterization.

Table 5-4. 386™SL CPU I_{CC} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC}	Supply Current				(Note 1)
	Minimum Configuration		400	mA	(Notes 2, 4)
	Maximum Configuration		750	mA	(Notes 3, 4)
I_{CC1}	Supply Current/Stop Clock		75	mA	(Notes 5, 6)
I_{CC2}	Supply Current/Suspend Mode/Oscillators Free Running/Suspend Refresh ON		10	mA	(Notes 5, 7)
I_{CC3}	Supply Current/Suspend Mode/Oscillators OFF Running/Suspend Refresh ON		6	mA	(Note 8)
I_{CC4}	Supply Current/Suspend Mode/Oscillators OFF Running/Suspend Refresh OFF		5	mA	(Note 9)

NOTES:
1. Tested at EFI and ISACLK2 at maximum frequency, with 50 pF load and no resistive loads on the outputs.
2. Minimum System Configuration consists of 1 bank of 1 Megabyte x 4 DRAMs (2 Megabyte total memory), cache disabled with no cache SRAM, 25 pF capacitive loading on the PI-bus control/status signals, 100 pF capacitive loading on the ISA-bus, 100 pF loading on the SYSCLK.
3. Maximum System Configuration consists of 4 banks of 4 Megabyte x 1 DRAMs (32 Megabytes total), cache enabled with 2 x (16k x 16) cache SRAMs, 65 pF capacitive loading on the PI-bus control/status signals, 300 pF capacitive loding (8 slots) on the ISA-bus and 300 pF capacitive loading on the SYSCLK signal.
4. Not tested, very conservative estimates provided from engineering analysis at worst case temperature and at 5.5V with the described system configuration for comparison only.
5. Characterized with V_{CC} = 5.5V, EFI = 40 MHz, ISACLK2 = 16 MHz
6. 412.5 mW with 386 SL CPU with Stop Clock, all external oscillators are free running, there are no active bus cycles on the Cache, Memory or ISA busses. Internal logic such as the Cache and Memory Controller are unaffected by stopped or slow clock and continue to consume the fixed power represented in I_{CC1}.
7. 55 mW with 386 SL CPU in suspend mode, all external oscillators are free running, there are no active bus cycles on the Cache, Memory or ISA busses except suspend refresh.
8. 33 mW with 386 SL CPU in suspend mode, all external oscillators are off (fixed Logic State), there are no active bus cycles on the Cache, Memory or ISA busses except suspend refresh.
9. 27.5 mW with 386 SL CPU in suspend mode, all external oscillators are off (fixed Logic State), there are no active bus cycles on the Cache, Memory or ISA busses including suspend refresh.

386™ SL CPU I_{CC} Specifications: Special Topics

DETERMINING I_{CC} WITH SLOW CLOCK CONTROL

The 386 SL CPU supports CPU clock division which reduces power consumption of the CPU core logic. The EFI clock input is similar to the CLK2 input found on the 386 CPU. However, the internal CPUCLK signal in the 386 SL CPU is not always one half of the frequency of the EFI (CLK2) input. An internal clock divider and synchronizer allows the CPU core clock to be slowed down and even stopped. However, additional internal logic such as the memory controller and cache controller continue to use half the EFI frequency. Therefore, when calculating the theoretical power consumption with CPU clock division it is important to recognize that a fixed constant (K) value of power is required by the 386 SL CPU.

The value K is constant only if the ISA bus loading is constant. Figure 5-1 shows the value of K for different values of ISA bus capacitance.

I_{CC}(divided clock) = [I_{CC}(normal clock) * n] + K

I_{CC}(normal clock) = The I_{CC} value calculated from the following section, excluding ISA bus power.

n = The fractional value that the clock is divided (e.g., divide by 2 = 0.5)

K = Is a constant in MilliAmps which determined by reading the value in Figure 5-1.

To determine the maximum current for the 386 SL CPU with CLK2 divider perform the following steps:

1. Multiply the I_{CC} of the normal minimum system configuration by the fractional value of the clock divider.
2. Sum the total capacitive load of all active ISA bus output signals from the 386 SL CPU to all devices.
3. From Figure 5-1 draw a line from the horizontal axis (capacitance) where it intersects the diagonal line.
4. From Figure 5-1 draw a perpendicular line to the vertical axis to determine K.
5. Solve the equation for I_{CC} (divided clock).

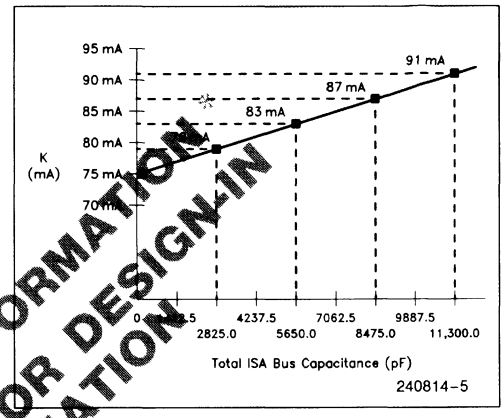


Figure 5-1. Variation of the constant current (K) with respect to the total ISA bus capacitance

I_{CC} WITH STOPPED CLOCK

Table 5-3. I_{CC} Static

Symbol	Parameter	Min	Max	Unit	Notes
I_{CCS}	Supply Current (static)	0	5	mA	(Note 1)

NOTE:
1. Tested while clock stopped in PH2 and inputs at V_{CC} or V_{SS} with the outputs unloaded. Clock stopped after IO Read at address 25H. EFI and ISACLK2 inputs should be at V_{CC} or V_{SS}.

POWER VARIATIONS WITH CAPACITIVE LOADS AT VARIOUS VOLTAGES

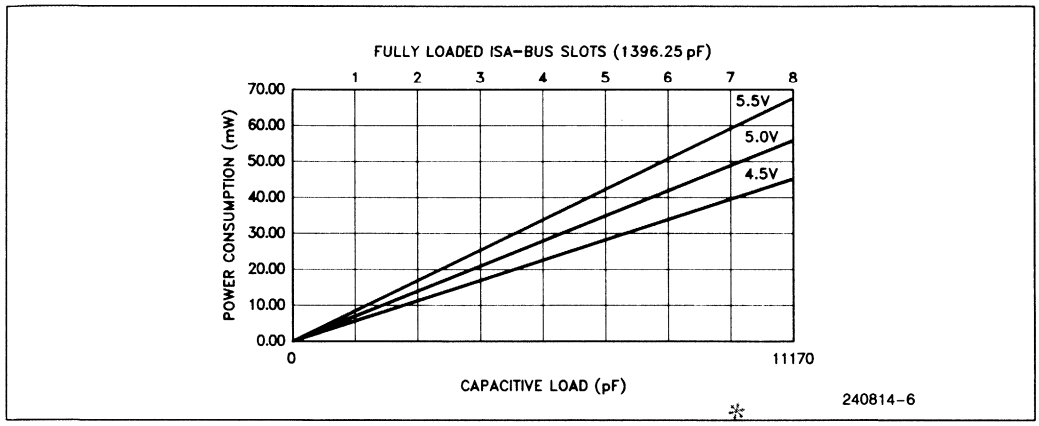


Figure 5-2. ISA Bus

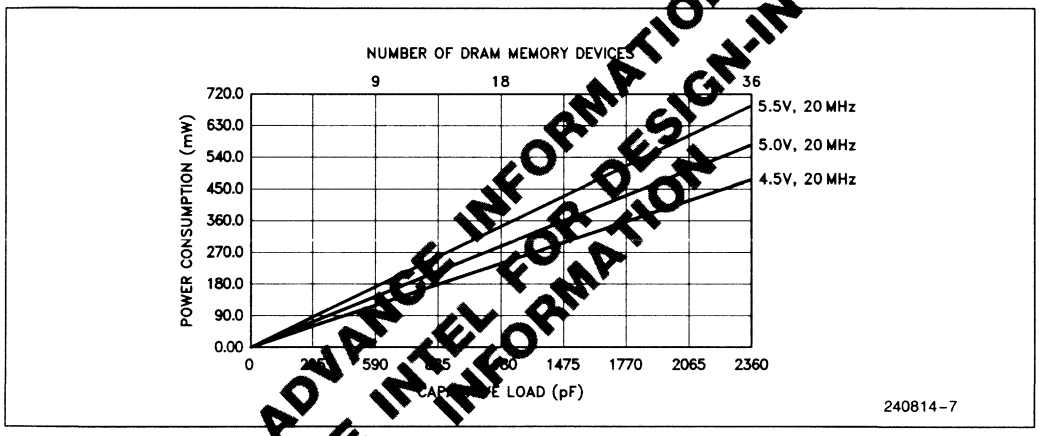


Figure 5-3a. Memory Bus without Cache

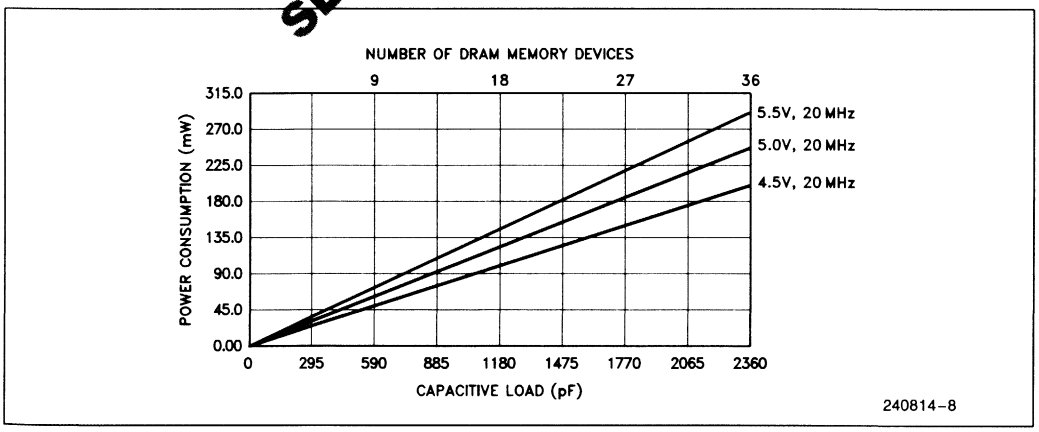


Figure 5-3b. Memory Bus with Cache

Calculation of I_{CC} for Various SL SuperSet System Configurations

A set of three curves with V_{CC} at 4.5V, 5V and 5.5V are plotted in Figure 5-2. Figure 5-2 illustrates the power consumption in milliWatts with respect to the capacitive loading on the ISA bus signals of the 386 SL CPU. The CPUCLK is assumed to be 20 MHz and EFI input is 40 MHz. A similar set of curves are provided for the memory bus without a cache subsystem in Figure 5-3a. The power consumption with respect to load capacitance for the memory bus with a cache subsystem is illustrated in Figure 5-3b. To find the Power (P in milliWatts) of the 386 SL CPU for the configuration of your system, use the following method.

1. Prepare a configuration list for your system including how many ISA-bus connectors, how many memory chips will be provided and whether a cache will be connected or not.
2. From the curves in Figure 5-2, use the voltage of your system and the total capactive load of all of the 386 SL CPU ISA signals to find the power consumed by the ISA-bus interface.
3. If a cache is connected to the 386 SL CPU in your system, use Figure 5-3b to find memory bus power. If cache is not connected, use Figure 5-3a.
4. Find the internal power consumption of the 386 SL CPU from Table 5-4 and the cache internal power and cache bus power from Tables 5-5 and 5-6.
5. For a system with no cache, add the ISA-bus interface power, the memory bus interface power without cache and the internal power. This gives the power consumption of the 386 SL CPU without cache.
6. For a system with cache, add the ISA bus interface power, the memory interface power with cache, the cache internal power, the cache bus interface power and the internal power. This gives the power consumption of the 386 SL CPU with cache.

Table 5-4. Internal Power

Frequency (MHz)	Power (mW)
20	1758.0

Table 5-5. Cache Bus Power (mW)

Freq. (MHz)	4.5V	5.0V	5.5V
20	24.71	30.5	36.91

Table 5-6. Cache Internal Power

Frequency (MHz)	Power (mW)
20	650

As an example, the power consumed by the 386 SL CPU when it is used in a 20 MHz system with 8 memory chips and 2 fully loaded ISA bus expansion slots will be calculated. The system voltage is assumed to be 5V.

From Figure 5-2, the power consumed by the ISA expansion bus interface is found to be 15 mW (the total capacitance of all the pins of a fully loaded AT-bus slot is 1396.25 pF). For a system with no cache, the power consumed by the memory bus for 8 chips is about 140 mW from Figure 5-3a. The internal power at 20 MHz is 1758.0 mW from Table 5-4. The power consumed by 386 SL CPU is the sum of the power for the internal power (ISA bus and CPU core) and memory bus. The total power consumed by the 386 SL CPU for this system is 1913 mW.

For a system with cache, the ISA bus interface power is 15 mW as previously determined. The memory bus interface power is determined from Figure 5-3b is found to be 60 mW. The internal power remains 1758.0 mW. The cache bus power is read off from Table 5-5 to be 30.5 mW and the cache internal power from table 5.6 is 650 mW. Hence, in this system, the 386 SL CPU consumes a total of 2513.5 mW.

82360SL D.C. Specifications

Functional operating range: V_{CC} = 5.0V ±10%, T_{CASE} = 0°C to 90°C.

Table 5-7. 82360SL D.C. Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	0.8	V	
V_{IH}	Input High Voltage	2.0 V_{CC} − 0.3	V_{CC} + 0.3	V V	 (Note 2)
I_{LI}	Input Leakage Current		±15	μA	(Note 1)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		15	pF	
C_{OUT}	Output or I/O Capacitance		15	pF	
I_{CCS1}	Suspend with Slow Refresh		50		(Note 9)
I_{CCS2}	Suspend without Slow Refresh		50	μA	(Note 9)
I_{CC}	Power Supply Current		180	mA	(Note 10)
D.C. Specifications for Standard ISA Bus Signals					
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 24 mA(4)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −3.3 mA(4)
D.C. Specifications for Parallel Port					
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 8 mA(3)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA(3)
D.C. Specifications for Open Drain Outputs					
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 24 mA(5) I_{OL} = 12 mA(6) I_{OL} = 16 mA(11)
D.C. Specifications for All Other Outputs					
V_{OL}	Output Low Voltage		0.5	V	I_{OL} = 12 mA(7)
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA(7)
D.C. Specifications for Power-Down Mode					
V_{BATT}	Battery Supply Voltage	3.0		V	
I_{BATT}	Battery Supply Current		100 50	μA μA	V_{BATT} = 5V V_{BATT} = 3.0V(8)

NOTES:
1. No pullup or pulldown.
2. For inputs—COMX1, CX1, RTCX1
3. For outputs—LPTD7:0
4. For outputs—OSC, AEN, SA16:0, LA23:17, MEMR#, MEMW#, IOR#, IOW#, SMEMW#, SMEMR#, SBHE#, TC, SD7:0, XD7, HD7, RESETDRV.
5. 0WS#, IOCHRDY, REFRESH#.
6. LPTSTROBE#, LPTAFD, LPTINIT#, LPTSLCTIN#, LPTDIR.
7. For all other outputs of the module.
8. Measured at V_{CC} = 0V, V_{BATT} = 3.0V, 32 kHz RTC clock with input rise time and fall time, $t_r = t_f < 50$ ns.
9. RTC clock at 32 kHz; Timer Clock, Serial clock and SYSCLK stopped; V_{CC} = 5.5V and RTCVCC = 5.5V, C_L = 50 pF with outputs unloaded.
10. I_{CC} tests at maximum frequency with no resisitive loads on the outputs.
11. REFRESH#

6.0 SL SuperSet TIMING SPECIFICATIONS

386 SL CPU A.C. Specifications

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
General: 20 MHz						
Ct 101	Qt1	EFI Period	25	500	ns	QNT1
Ct 102a	Qt2a	EFI High Time at 2V	8		ns	
Ct 102b	Qt2b	EFI High Time at 3.7V	5		ns	
Ct 103a	Qt3a	EFI Low Time at 2V	8		ns	
Ct 103b	Qt3b	EFI Low Time at 0.8V	6 *		ns	
Ct 104	Qt4	EFI Fall Time from (V_{CC} − 0.8V) to 0.8V		8	ns	
Ct 105	Qt5	EFI Rise Time 0.8V to (V_{CC} − 0.8V)		8	ns	
Ct 111		PWRGOOD Minimum Pulse Width	1		EFI	
Ct 111a	Qt21a	PWRGOOD Setup to EFI	12		ns	QNT3
Ct 111b	Qt21b	PWRGOOD Hold Time	4		ns	
Ct 112		CPURESET Minimum Pulse Width	1		EFI	
Ct 112a	Qt22a	CPURESET Setup to EFI	12		ns	QNT3
Ct 112b	Qt22b	CPURESET Hold Time	4		ns	
Ct 113		STPCLK# Minimum Pulse Width	2		EFI	
Ct 113a	Qt23a	STPCLK# Setup to EFI	15		ns	QNT3
Ct 113b	Qt23b	STPCLK# Hold Time	20		ns	
Ct 114a	Qt24a *	SUS_STAT# Setup to EFI	20		ns	QNT3
Ct 114b	Qt24b	SUS_STAT# Hold Time	15		ns	
Ct 115		ONCE# Minimumimum Pulse Width	35		ns	
Ct 115a	Qt25a	ONCE# Setup to EFI	20		ns	QNT3
Ct 115b	Qt25b	ONCE# Hold Time	15		ns	
Ct 116a	Nt2a	SMI# Setup to EFI	15		ns	QNT3
Ct 116b	Nt2b	SMI# Hold Time	21		ns	
Ct 117a	Xtla	INTR Setup to EFI	15		ns	QNT3
Ct 117b	Xtlb	INTR Hold Time	45		ns	
Ct 118a	Xt2a	NMI Setup to EFI	11		ns	QNT3
Ct 118b	Xt2b	NMI Hold Time	16		ns	

NOTES:
QNT1. EFI maximum period is specified only for the case where a MCP (Math co-processor) is present in the system. NPXCLK period, high and low time are tested at 2V. All other parameters are guaranteed by design characterization.
QNT3. A20GATE, CPURESET, INTR, NMI, ONCE#, PWRGOOD, SMI#, STPCLK# and SUS_STAT# are asynchronous inputs to the 386 SL CPU. Setup and hold times with respect to the EFI input are provided for test purposes only. The minimum setup and hold times are specified for valid recognition at a specific clock edge. The minimum valid pulse width can be extrapolated from the setup and hold times with respect to EFI.

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
ISA-Bus Clock Timings						
Ct 201	Qt31	ISACLK2 Period	62.5		ns	QNT4
Ct 202	Qt32	ISACLK2 High Time at 2V	28	32.5	ns	QNT4
Ct 203	Qt33	ISACLK2 Low Time at 2V	28	32.5	ns	QNT4
Ct 204	Qt34	ISACLK2 Fall Time from (V_{CC} − 0.8V) to 0.8V	*	8	ns	QNT4
Ct 205	Qt35	ISACLK2 Rise Time from 0.8V to (V_{CC} − 0.8V)		8	ns	QNT4
Ct 206	Qt36	ISACLK2 to SYSCLK Delay, Falling to Rising Edge		32	ns	
Ct 211	Qt41	SYSCLK Period	125		ns	QNT5
Ct 212	Qt42	SYSCLK High Time at 2V	53		ns	QNT5
Ct 213	Qt43	SYSCLK Low Time at 2V	57		ns	QNT5
Ct 214	Qt44	SYSCLK Fall Time from (V_{CC} − 0.8V) to 0.8V		10	ns	QNT5
Ct 215	Qt45	SYSCLK Rise Time from 0.8V to (V_{CC} − 0.8V)		10	ns	QNT5
Ct 272a	Nt1a	A20GATE Setup to EEC(HTT)	11		ns	QNT3
Ct 272b	Nt1b	A20GATE Hold Time	21		ns	
ISA-Bus Timings *						
Ct 221	G7	BALE Active Delay from T_S phi 2 Low		52	ns	Nt1
Ct 222	G8	BALE Inactive Delay from T_C phi 1 Low	8	47	ns	
Ct 223	G9	LA17–23 Valid Delay from T_C or T_C phi 2 Low		34	ns	
Ct 224	G10	LA17–23 Invalid Delay from T_C phi 2 Low	0		ns	

NOTES:
QNT4. ISACLK2 minimum period, high and low times are specified with ISACLK2 input = 16 MHz and SYSCLK output = 8 MHz. The ISACLK2 input specifications are provided to ensure that the SYSCLK output, period, minimum high and low time, rise and fall time and ISACLK2 to SYSCLK skew are met.
QNT5. SYSCLK capacitive loading is 20 pF minimum and 120 pF maximum. SYSCLK period, low and high time are tested at 1.5V thresholds. All other parameters are guaranteed by design characterization.

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
ISA-Bus Timings (Continued)						
Ct 225	G13	SA1–19 Valid Delay from T_S phi 2 Low		56	ns	
Ct 226	G13a	SA0–19, SBHE#, LA17–23 Valid Setup to phi 1 Low (External Master)	18		ns	
Ct 227	G14	SA1–19 Invalid Delay from T_S phi 2 Low	0	45	ns	
Ct 228	G15	SA0, SBHE# Valid Delay from T_S phi 2 Low		52	ns	
Ct 229	G16	SA0, SHBE# Float Delay from T_S phi 1	0	45	ns	
Ct 230	G17	MEMR#, MEMW# Active from T_C phi 1 Low (16-bit Memory Cycles)	7	45	ns	
Ct 231	G17a	Command Active Setup to phi 1 Low (External Master)	17.5		ns	
Ct 232	G17b	HALT# Valid Delay from phi 1 Low		34	ns	NT8
Ct 233	G18	Command Inactive to Float Delay from TI phi 1 Low (External Master)		45	ns	
Ct 234	G19	Command Active Delay from T1 phi 2 Low (IOR#/IOW# 8 or 16-bit, MEM#/MEMW# 8-bit)	7	45	ns	
Ct 235	G20	Command Inactive Delay from Teoc phi 1 Low (MEMR#/MEMW#, IOR#/IOW# and HALT#)		45	ns	NT2
Ct 238	G23	MEMCS16# Setup to T_C phi 1 Low	0		ns	NT6, NT12
Ct 239	G24	MEMCS16# Hold from T_C phi 1 Low	10		ns	NT6; NT12
Ct 240	G25	IOCS16# Setup to T_C phi 2 Low	2		ns	NT7
Ct 241	G26	IOCS16# Hold from Teoc phi 1 Low	0		ns	NT7
Ct 242	G27	ZEROWS# Setup to T_C phi 2 Low	0		ns	NT7, NT9
Ct 244	G29	ZEROWS# Hold from T_C phi 2 Low	10		ns	NT7, NT9
Ct 245	G29a	MEMCS16# Active Delay from Valid Address (External Master Cycles)		64	ns	
Ct 246	G30	SD0–15 Valid Setup to Teoc phi 1 Low	18		ns	Ext. Master
Ct 247	G31	SD0–15 Hold from Teoc phi 1 Low	16		ns	Read Cycle, NT10
Ct 248	G32	SD0–7 Valid Delay from T_S phi 2 Low	30	65	ns	Write Cycle
Ct 249	G33	SD8–15 Valid Delay from T_S phi 2 Low	37	65	ns	Write Cycle
Ct 250	G34	SD0–15 Invalid Delay from Teoc phi 1 Low	4		ns	Write Cycle

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
ISA-Bus Timings (Continued)						
Ct 251	G35	IOCHRDY Setup to T_C phi 2 Low	0		ns	
Ct 252	G36	IOCHRDY Hold from T_C phi 2 Low	8		ns	NT11
Ct 255	G39	NMI/SMI# Setup to Tx phi 2 Low	16			Asynch
Ct 256	G40	NMI/SMI# Hold from Tx phi 2 Low			bs	Asynch
Ct 257	G41	INTR Setup to Tx phi 2 Low	45		ns	Asynch, NT4
Ct 258	G42	INTR Hold from Tx phi 2 Low			ns	Asynch
Ct 259	G43	INTA Active Delay from T_C phi 2 Low		45	ns	NT16
Ct 260	G44	INTA Inactive Delay from Teoc phi 1 Low		60	ns	NT17
Ct 261	G45	HRQ Setup to T_C or Ti phi 2 Low			ns	
Ct 262		HRQ Hold from Th phi 2 Low			ns	
Ct 263	G48a	HLDA Active Delay from Th phi 1 Low			ns	NT3 C_L = 65 pF
Ct 264	G48b	HLDA Inactive Delay from Th phi 1 Low		38	ns	C_L = 65 pF
Ct 265	G49	DMA8/16# Setup to Th phi 2 Low	15		ns	NT13, NT14, NT15
Ct 266	G50	MASTER# Setup to Th phi 2 Low			ns	NT15
Ct 267	G51	REFREQ Setup to Ti or Th phi 2 Low	15		ns	
Ct 268	G53c	VGACS# Active Delay from LA[23:17]		35	ns	
Ct 269	G53d	VGACS# Inactive Delay from LA[23:17]		35	ns	
Ct 270	G54a	ROMCS0#/CMUX14# Active Delay from T_S phi 2 Low		48	ns	NT18
Ct 271	G54b	ROMCS0#/CMUX14# Inactive Delay from T_S phi 2 Low		48	ns	NT18
Ct 272	G54c	ROMCS0#/CMUX14# Active Delay from LA[23:17]		41	ns	NT19
Ct 273	G54d	ROMCS0#/CMUX14# Inactive Delay from LA[23:17]		41	ns	NT19
Ct 274	G55a	SMRAMCS# Active Delay from T_S phi 2 Low	10	49	ns	NT18
Ct 275	G55b	SMRAMCS# Inactive Delay from T_S or Ti phi 2 Low	10	49	ns	NT18
Ct 271	G56	TURBO Setup	16		ns	Asynch

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
ISA-Bus Timings (Continued)						
Ct 276		SD15–0 Valid Delay from IOCHRDY Asserted (External Master)		48	ns	
Ct 277		SD15–0 Data Invalid Delay from MEMR# Inactive (External Master)	7		ns	
Ct 278		SD15–0 Data Invalid Delay from IOR# Inactive (External Master)	7		ns	
Ct 279		SD15–0 Data Setup to MEMW# Active (External Master)	0		ns	
Ct 280		SD15–0 Data Hold from MEMW# Inactive (External Master)	0		ns	
Ct 281		SD15–0 Setup to IOW# Active (External Master)	0		ns	
Ct 282		BALE Active Delay from Th phi 1 Low (External Master)		45	ns	
Ct 283		BALE Inactive from Th phi 1 Low (External Master)		45	ns	
Ct 284		LA23–17, SA19–0, SBHE# Float to Invalid Delay from Th phi 2 (External Master)		54	ns	
Ct 285		LA23–17, SA19–0, SBHE# Invalid to Float Delay from Th phi 1 (External Master)		54	ns	
Ct 286		SA19–17 Delay from SA19–0 (External Master)	10	45	ns	
Ct 287		Command Float to Inactive from Th phi 2 Low (External Master)		45	ns	
Ct 288		Address Setup to Command Active (External Master)	40		ns	
Ct 289		SA15–0 Hold after IOR# or IOW# Inactive (External Master)	15		ns	
Ct 290		IOCS16# Active Delay from Valid Address (External Master)		52	ns	
Ct 291		SD15–0 Delay from IOR# Active (External Master) Read from CPU I/O Ports)		65	ns	
Ct 292		SD15–0 Valid Delay from phi 2 Low (External Master) Read from On Board Memory)		95	ns	Test Only
Ct 293		SD15–0 Hold from IOW# Inactive (External Master)	15		ns	
Ct 294		Byte Swap Delay (External Master)	10	72	ns	NT5

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
ISA-Bus Timings (Continued)						
Ct 295		IOCHRDY Invalid from Command Active (External Master)		105	ns	
Ct 296		IOCHRDY Active Delay from phi 2 Low (External Master)		85	ns	Test Only
Ct 297		IOCHRDY Inactive from MEMR# Active (External Master Accessing ROM)		44	ns	

NOTES:

NT1. The ISA bus timings are specified in a synchronous manner with respect to the ISACLK2 input. ISACLK2 input is 16 MHz, which is twice the frequency of the SYSCLK output. Each SYSCLK period represents one T-state and each T-state corresponds to either the beginning of a bus cycle (T_S—Send Status), middle of a bus cycle (T_C—execute command), end of cycle (T_{eoc}), hold (T_h) or idle (T_i). T-States, (T_S, T_C, T_{eoc}, T_h, T_i) are comprised of two ISACLK2 periods (Phi 1 and Phi 2). The ISACLK2 Periods or Phases, (Phi 1 and Phi 2), falling or rising edge are used to reference the synchronous ISA parameters. ISACLK2 Phi 1 falling edge leads SYSCLK rising edge, ISACLK2 Phi 2 falling edge leads SYSCLK falling edge.

NT2. T_{eoc} represents the End of Cycle. The falling edge of ISACLK2 Phi 2 during T_C indicates T_{eoc}.

NT3. After HLDA (Hold Acknowledge) is de-asserted, the 386 SL CPU drives the address bus with the previous address that was latched prior to the beginning of the HLDA cycle. The term "invalid" refers to this latched address. The latched address may or may not be valid for the next CPU bus cycle. The start of the next CPU bus cycle on an external bus a valid address will be placed on the address bus.

NT4. INTR, NMI, SMI#, and TURBO are asynchronous inputs with respect to ISACLK2 and SYSCLK. These are input signals to the 386 SL CPU. Setup and hold times with respect to the ISACLK2 input are provided for reference. The minimum setup and hold times are specified for valid recognition at a specific clock edge in other timing diagrams with the EFI clock input.

NT5. The setup time is required to ensure that byte swapping is not delayed when an external master reads from an 8-bit device on an odd byte address boundary.

NT6. MEMCS16# is sampled on the falling edge of ISACLK2 Phi 2.

NT7. IOCS16# and ZEROWS# are sampled on the falling edge of ISACLK2 Phi 1.

NT8. HALT timing is identical to a 16-bit AT bus cycle at memory bus cycle except that no BALE or Status Signal is asserted.

NT9. ZEROWS# and IOCHRDY should not be active during LOW during the same bus cycle.

NT10. SD0–15 read data is sampled on the falling edge of ISACLK2 Phi 2 at T_{eoc} (End of Cycle).

NT11. IOCHRDY de-asserted (LOW) is sampled on the falling edge of ISACLK2 Phi 2 when Command is active (LOW). De-asserting IOCHRDY# adds incremental wait states (1 SYSCLK long). IOCHRDY should not be held LOW longer than 17 SYSCLKs (2.1 μs.).

NT12. ROM read bus cycles are similar to 8/16 bit ISA bus memory read bus cycles except that MEMCS# is ignored. The strapping pin ROM16/8# is sampled to determine if the ROM read is an 8-bit or 16-bit memory read. Additionally ROMCS0# and/or ROMCS1# are asserted during a ROM read.

NT13. DMA bus cycles are not supported to On-board I/O ports. AEN is HIGH during MASTER, DMA and access to the configuration registers.

NT14. Byte swap timing for 8-bit DMA bus cycles is identical to that of an external master.

NT15. During DMA cycles the 386 SL CPU drives SA17–19 with the value of LA17–19 while HLDA is active. During other Slave cycles (i.e., Refresh and External Master) the 386 SL CPU does not drive SA17–19.

NT16. During the INTA# cycle, SD8–15 should not change state. During the first INTA# pulse SD0–15 are ignored. The second INTA# pulse in an INTA# bus cycle indicates a bus cycle that is similar to an 8-bit I/O read in which the interrupt vector is read from SD0–7.

NT17. The 8259 INTA# minimum pulse width is 160 ns.

NT18. ROMCS0#, ROMCS1# and SMRAMCS# are specified with respect to ISACLK2 when the CPU is the bus master.

NT19. ROMCS0#, ROMCS1# and SMRAMCS# are specified with respect to valid address when an external master controls the bus.

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
PI-Bus Timings: 20 MHz						
Ct 301		Min. Chip Select and Command Setup to PSTART# Active	30		ns	
Ct 302		Min. Chip Select and Command Hold from PSTART# Active	50		ns	
Ct 303		Max. PRDY# Hold Time after PCMD# Inactive		72	ns	
Ct 304		Min. Read Data Setup Time to PCMD# Inactive	30		ns	
Ct 305		Min. Read Data Hold Time from PCMD# Inactive	9		ns	
Ct 306		Min. PRDY# Active Delay from PSTART# Active	94		ns	
Ct 307		Maximum Write Data Valid Delay from PSTART# Active	*	54	ns	
Ct 308		Min. Write Data Invalid Delay from PCMD# Inactive	27		ns	
Ct 309		Min Address Setup Time to PSTART# Active	30		ns	
Ct 310		Min Address Hold Time from PSTART# Active	58		ns	
Ct 311		PSTART# Pulse Width	50		ns	
Ct 312		Min Delay from PSTART# Active to PCMD# Active	50		ns	
Ct 313		Min Delay from PRDY# Active to PCMD# Inactive	32		ns	
Ct 314		Min Delay from PCMD# Inactive to PSTART# Active	50		ns	
External Master Timings: SYSCLK at 8 MHz (Slave CPU)						
Ct 321	t1s	PW/RD# Valid Delay		35	ns	ATCLK2 Sync.
Ct 321	t1s	M/IO# Valid Delay		35	ns	ATCLK2 Sync.
Ct 321	t1s	VGACS# Valid Delay		35	ns	ATCLK2 Sync.
Ct 325	t3s	PSTART# Valid Delay		24	ns	ATCLK2 Sync.
Ct 326	t4s	PCMD# Valid Delay		24	ns	ATCLK2 Sync.
Ct 327a	t5as	PRDY# Set-up	5		ns	ATCLK2 Sync.
Ct 327b	t5bs	PRDY# Hold	25		ns	ATCLK2 Sync.
CPU Master						
Ct 328	t2s	SA[1:16] Valid Delay				Tri-Stated
Ct 328	t2s	SA[17:19] Valid Delay				Tri-Stated
Ct 328	t2s	LA[17:23] Valid Delay				Tri-Stated
Ct 328	t2s	SBHE#, SAO Valid Delay				Tri-Stated
Ct 332	t6s	SD[0:15] Valid Delay				Tri-Stated

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
CPU Master (Continued)						
Ct 341		PW/R#, PM/IO#, VGACS# Valid Delay from EFI T1 phi 1 High		53	ns	(Note 3)
Ct 342		SA[19:0], LA[23:17], SBHE# Valid Delay from EFI T1 phi 1 High		63	ns	
Ct 343a		PSTART# Active (LOW) Delay from EFI T2 phi High		33	ns	
Ct 343b		PSTART# Inactive (HIGH) Delay from EFI T2 phi 2 Low		33	ns	
Ct 344a		PCMD# Active (LOW) Delay from EFI T2 phi 1 High		33	ns	
Ct 344b		PCMD# Inactive (HIGH) Delay from EFI T2 phi 2 Low		33	ns	
Ct 345a		PRDY# Setup to EFI T2 phi 1 Low (CPU is Bus Master)	0		ns	
Ct 345b		PRDY# Hold from EFI T2 phi 2 Low (CPU is Bus Master)	25		ns	
Ct 347a		SD[15:0] Setup to EFI T2 phi 2 Low (CPU Read from PI Bus Slave Device)	21		ns	(Note 7)
Ct 347b	✳	SD[15:0] Hold from EFI T2 phi 2 Low (CPU Read from PI Bus Slave Device)	15		ns	
Ct 348		SD[15:0] Valid Delay from EPI T2 phi 2 High (CPU Write to PI Bus Slave Device)		62	ns	

NOTES:
1. VGACS#, FLSHDCS#, PW/R#, PM/IO# and Addresses change for each subsequent read or write.
2. PSTART# indicates a new cycle in which address, status and chip selects are valid before PSTART# is asserted LOW. PRDY# terminates each bus cycle and a new PSTART# is driven if a new address and status signals are available.
3. EFI = 50 MHz, Internal CPU Phase CLK = 25 MHz.
4. ISACLK2 = 16 MHz.
5. Maximum parameters are based on worst case condition of V_{CC} = 4.2V, 120°C.
6. Minimum parameters are based on best case condition of V_{CC} = 5.6V, 10°C.
7. PRDY# setup worst case condition is −4 ns, 0 ns specified for test purposes.

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
Cache Bus Timings: 20 MHz						
Ct 401	t1	CABUS Setup to COE# Active Low	−1		ns	HNT1
Ct 402	t2	COE# Puslse Width	72		ns	HNT2
Ct 403	t3	CCSH#, CCSL# Active to COE# Active	1		ns	HNT3
Ct 404a	t4	CDBUS Setup to COE# Active	36		ns	HNT4
Ct 404b		CDBUS Hold from COE# Active	3		ns	
Ct 405	t5	CABUS Valid to CWE# Inactive High	96		ns	
Ct 406	t6	CWE# Active Width	35		ns	
Ct 407	t7	CDBUS Setup to CWE# Inactive	25		ns	
Ct 408	t8	CDBUS Hold to CWE# Inactive	0		ns	
Ct 409	t9	CABUS Hold to CWE# Inactive	6		ns	
Math Coprocessor Timings: 20 MHz						
Ct 421	Ht11	CA2 Valid Delay (NPX Cycle)	3	25	ns	HNT1
Ct 422	Ht12	NPXADS# Valid Delay	5	27	ns	HNT5
Ct 423	Ht13	NPXW/R# Valid Delay	5	27	ns	HNT5
Ct 424	Ht14	CD Valid Delay (NPX Cycle)	2	35	ns	HNT4
Ct 425a	Ht15a	NPXRDY# Setup	16		ns	
Ct 425b	Ht15b	NPXRDY# Hold	3		ns	
Ct 426a	Ht16a	BUSY#, PEREQ, ERROR# Setup	14		ns	
Ct 426b	Ht16b	BUSY#, PEREQ, ERROR# Hold	5		ns	
Ct 427a	Ht17a	CD Setup (NPX Cycle)	12		ns	
Ct 427b	Ht17b	CD Hold (NPX Cycle)	6		ns	

NOTES:
QNT1. EFI maximum period is specified only for the case where a MCP (Math Co-processor) is present in the system. NPXCLK, period, high and low time at 2V are tested. All other parameters are guaranteed by design characterization.
QNT2. NPXCLK, NPXRESET Loading: 30 pF. (Timing specified here is for in-system loading, Timing Spec with Tester Loading is TBD.)
HNT1. CA Loading: min 10 pF, max 50 pF.
HNT4. CD Loading: min 10 pF, max 35 pF. (Timing specified here is for in-system loading, Timing Spec with Tester Loading is TBD.)
HNT5. NPXADS#, NPXW/R# Loading: 25 pF. (Timing specified here is for in-system loading, Timing Spec with Tester Loading is TBD.)

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
Math Coprocessor Timings: 20 MHz (Continued)						
Ct 441	Qt11	NPXCLK Period	25	500	ns	QNT1
Ct 442a	Qt12a	NPXCLK High Time 2V	6		ns	QNT2
Ct 442b	Qt12b	NPXCLK High Time 3.7V	3		ns	
Ct 443a	Qt13a	NPXCLK Low Time 2V	6		ns	
Ct 443b	Qt13b	NPXCLK Low Time 0.8V	4		ns	
C t 444	Qt14	NPXCLK Fall Time (V_{CC} − 0.8V) to 0.8V		8	ns	
Ct 445	Qt15	NPXCLK Rise Time 0.8V to (V_{CC} − 0.8V)		8	ns	
Ct 446	Qt26	NPXCLK - Delay from RESET - NPXCLK			ns	
SRAM Mode: 20 MHz Timings						
Ct 501	tOAC	Access Time from OE#			ns	2 Wait State
Ct 502	tOAC	Access Time from OE#	50		ns	3 Wait State
Ct 503	tCSD	CE# Setup to OE# Active			ns	2 Wait State
Ct 504	tCSD	CE# Setup to OE# Active	50		ns	3 Wait State
Ct 505	tASD	Addr Setup to OE# Active	40		ns	2 Wait State
Ct 506	tASO	Addr Setup to OE# Active	50		ns	3 Wait State
Ct 507	tCSW	CE# Setup to WE# Active	0		ns	2 Wait State
Ct 508	tCSW	CE# Setup to WE# Active	0		ns	3 Wait State
Ct 509	tASW	Addr Setup to WE# Active	0		ns	2 Wait State
Ct 510	tASW	Addr Setup to WE# Active	0		ns	3 Wait State
Ct 511	tWP	WE# Active Pulse Width	70		ns	2 Wait State
Ct 512	tWP	WE# Active Pulse Width	90		ns	3 Wait State
Ct 513	tWR	WE# Recovery Time	10		ns	2 Wait State
Ct 514	tWR	WE# Recovery Time	10		ns	3 Wait State
Ct 515	tDS	Write Data Setup to WE# Inactive	35		ns	2 Wait State
Ct 516	tDS	Write Data Setup to WE# Inactive	40		ns	3 Wait State
Ct 517	tDH	Write Data Hold from WE# Inactive	0		ns	2 Wait State
Ct 518	tDH	Write Data Hold from WE# Inactive	0		ns	3 Wait State

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
SRAM Mode: 20 MHz Timings (Continued)						
Ct 519	tDSO	DIR Setup to OE# Active	0		ns	2 Wait State
Ct 520	tDSO	DIR Setup to OE# Active	0		ns	3 Wait State
Ct 521	tDHO	DEN# Hold from OE# Inactive	0		ns	2 Wait State
Ct 522	tDHO	DEN# Hold from OE# Inactive	0		ns	3 Wait State
Ct 523	tOSD	OE# Inactive Setup to DEN# Active	30		ns	2 Wait State
Ct 524	tOSD	OE# Inactive Setup to DEN# Active	40		ns	3 Wait State
Ct 525	tDSW	DIR Inactive Setup to WE# Active	0		ns	2 Wait State
Ct 526	tDSW	DIR Inactive Setup to WE# Active	0		ns	3 Wait State
Ct 527	tDHW	DEN# Hold from WE# Inactive	0		ns	2 Wait State
Ct 528	tDHW	DEN# Hold from WE# Inactive	0		ns	3 Wait State
Ct 529	tDSD	DIR Inactive Setup to DEN# Active	0		ns	2 Wait State
Ct 530	tDSD	DIR Inactive Setup to DEN# Active	0		ns	3 Wait State
Ct 531	tDRH	DIR Hold from DEN# Inactive	0		ns	2 Wait State
Ct 532	tDRH	DIR Hold from DEN# Inactive	0		ns	3 Wait State
Ct 533	tDRS	DIR Setup to DEN# Active	0		ns	2 Wait State
Ct 534	tDRS	DIR Setup to DEN# Active	0		ns	3 Wait State
Ct 535	tASL	Upper Addr Setup to LE Inactive	8		ns	2 Wait State
Ct 536	tASL	Upper Addr Setup to LE Inactive	8		ns	3 Wait State
Ct 537	tAHL	Upper Addr Hold from LE Inactive	0		ns	2 Wait State
Ct 538	tAHL	Upper Addr Hold from LE Inactive	0		ns	3 Wait State
Ct 539	tLP	LE Active Pulse Width	8		ns	2 Wait State
Ct 540	tLP	LE Active Pulse Width	8		ns	3 Wait State
Ct 541	tAVL	Addr Valid Delay from LE Inactive		50	ns	2 Wait State
Ct 542	tAVL	Addr Valid Delay from LE Inactive		70	ns	3 Wait State

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
DRAM Mode: 20 MHz Timings						
Ct 601	tASR	Row Addr Setup to RAS# Active	0		ns	F1 Mode
Ct 602	tASR	Row Addr Setup to RAS# Active	0		ns	F2 Mode
Ct 603	tASR	Row Addr Setup to RAS# Active	0		ns	P1 Mode
Ct 605	tRAH	Row Addr Hold from RAS# Active	12		ns	F1 Mode
Ct 606	tRAH	Row Addr Hold from RAS# Active	12		ns	F2 Mode
Ct 607	tRAH	Row Addr Hold from RAS# Active	12		ns	P1 Mode
Ct 609	tASC	Col Addr Setup to CAS# Active	0		ns	F1 Mode
Ct 610	tASC	Col Addr Setup to CAS# Active	0		ns	F2 Mode
Ct 611	tASC	Col Addr Setup to CAS# Active	0		ns	P1 Mode
Ct 613	tCAH	Col Addr Hold from CAS# Active	15		ns	F1 Mode
Ct 614	tCAH	Col Addr Hold from CAS# Active	15		ns	F2 Mode
Ct 615	tCAH	Col Addr Hold from CAS# Active	20		ns	P1 Mode
Ct 617	tRCD	RAS# to CAS# Delay	20		ns	F1 Mode
Ct 618	tRCD	RAS# to CAS# Delay	20		ns	F2 Mode
Ct 619	tRCD	RAS# to CAS# Delay	20		ns	P1 Mode
Ct 621	tCSH	CAS# Hold Time from RAS# Active	80		ns	F1 Mode
Ct 622	tCSH	CAS# Hold Time from RAS# Active	100		ns	F2 Mode
Ct 623	tCSH	CAS# Hold Time from RAS# Active	100		ns	P1 Mode
Ct 625	tRSH	RAS# Hold Time from CAS# Active	20		ns	F1 Mode
Ct 626	tRSH	RAS# Hold Time from CAS# Active	20		ns	F2 Mode
Ct 627	tRSH	RAS# Hold Time from CAS# Active	30		ns	P1 Mode
Ct 629	tWCS	WE# Setup to CAS# Active (Write)	0		ns	F1 Mode
Ct 630	tWCS	WE# Setup to CAS# Active (Write)	0		ns	F2 Mode
Ct 631	tWCS	WE# Setup to CAS# Active (Write)	0		ns	P1 Mode
Ct 633	tWCH	WE# Hold from, CAS# Active (Write)	20		ns	F1 Mode
Ct 634	tWCH	WE# Hold from, CAS# Active (Write)	20		ns	F2 Mode
Ct 635	tWCH	WE# Hold from, CAS# Active (Write)	20		ns	P1 Mode
Ct 637	tRCS	WE# Setup to CAS# Active (Read)	0		ns	F1 Mode
Ct 638	tRCS	WE# Setup to CAS# Active (Read)	0		ns	F2 Mode
Ct 639	tRCS	WE# Setup to CAS# Active (Read)	0		ns	P1 Mode
Ct 641	tRCH	WE# Hold from CAS# Inactive (Read)	0		ns	F1 Mode
Ct 642	tRCH	WE# Hold from CAS# Inactive (Read)	0		ns	F2 Mode
Ct 643	tRCH	WE# Hold from CAS# Inactive (Read)	0		ns	P1 Mode
Ct 645	tWDS	Write Data Setup to CAS# Active	0		ns	F1 Mode

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
DRAM Mode: 20 MHz Timings (Continued)						
Ct 646	tWDS	Write Data Setup to CAS# Active	0		ns	F2 Mode
Ct 647	tWDS	Write Data Setup to CAS# Active	0		ns	P1 Mode
Ct 649	tWDH	Write Data Hold from CAS# Active	20		ns	F1 Mode
Ct 650	tWDH	Write Data Hold from CAS# Active	20		ns	F2 Mode
Ct 651	tWDH	Write Data Hold from CAS# Active	20		ns	P1 Mode
Ct 653	tRAC	Access Time from RAS# Active	80		ns	F1 Mode
Ct 654	tRAC	Access Time from RAS# Active	100		ns	F2 Mode
Ct 655	tRAC	Access Time from RAS# Active	100		ns	P1 Mode
Ct 657	tCAC	Access Time from CAS# Active	20		ns	F1 Mode
Ct 658	tCAC	Access Time from CAS# Active	20		ns	F2 Mode
Ct 659	tCAC	Access Time from CAS# Active	20		ns	P1 Mode
Ct 661	tRDH	Read Data Hold from CAS# Inactive	0		ns	F1 Mode
Ct 662	tRDH	Read Data Hold from CAS# Inactive	0		ns	F2 Mode
Ct 663	tRDH	Read Data Hold from CAS# Inactive	0		ns	P1 Mode
Ct 665	tRAS	RAS# Active Pulse Width	80	*	ns	F1 Mode
Ct 666	tRAS	RAS# Active Pulse Width	100	*	ns	F2 Mode
Ct 667	tRAS	RAS# Active Pulse Width	100	*	ns	P1 Mode
Ct 669	tCAS	CAS# Active Pulse Width	25		ns	F1 Mode
Ct 670	tCAS	CAS# Active Pulse Width	25		ns	F2 Mode
Ct 671	tCAS	CAS# Active Pulse Width	35		ns	P1 Mode
Ct 673	tRP	RAS# Precharge Pulse Width	70		ns	F1 Mode
Ct 674	tRP	RAS# Precharge Pulse Width	90		ns	F2 Mode
Ct 675	tRP	RAS# Precharge Pulse Width	110		ns	P1 Mode
Ct 677	tCP	CAS# Precharge Pulse Width	15		ns	F1 Mode
Ct 678	tCP	CAS# Precharge Pulse Width	15		ns	F2 Mode
Ct 679	tCP	CAS# Precharge Pulse Width	15		ns	P1 Mode
Ct 681	tPSW	PARx# Setup to CAS# Active (Write)	1		ns	F1 Mode
Ct 682	tPSW	PARx# Setup to CAS# Active (Write)	1		ns	F2 Mode
Ct 683	tPSW	PARx# Setup to CAS# Active (Write)	1		ns	P1 Mode
Ct 685	tPHW	PARx# Hold from CAS# Active (Write)	20		ns	F1 Mode
Ct 686	tPHW	PARx# Hold from CAS# Active (Write)	20		ns	F2 Mode
Ct 687	tPHW	PARx# Hold from CAS# Active (Write)	20		ns	P1 Mode
Ct 689	tPVR	PARx# Valid from CAS# Active (Read)	27		ns	F1 Mode
Ct 690	tPVR	PARx# Valid from CAS# Active (Read)	27		ns	F2 Mode

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

386 SL CPU A.C. Specifications (Continued)

Symbol	Alt Symbol	Parameter	Min *	Max	Unit	Notes
DRAM Mode: 20 MHz Timings (Continued)						
Ct 691	tPVR	PARx# Valid from CAS# Active (Read)	12		ns	P1 Mode
Ct 693	tPHR	PARx# Hold from CAS# Inactive (Read)	1		ns	F1 Mode
Ct 694	tPHR	PARx# Hold from CAS# Inactive (Read)			ns	F2 Mode
Ct 695	tPHR	PARx# Hold from CAS# Inactive (Read)	1		ns	P1 Mode
Parity Error						
Ct 701	tPED	PERR# Delay from SYSCLK		38	ns	
Ct 702	tCSR	CAS# Setup to RAS# Active (DRAM Refresh)	10		ns	
Ct 703	tCHR	CAS# Hold from RAS# Active (DRAM Refresh)	30		ns	
Ct 704	tWRP	WE# Setup to RAS# Active (DRAM Refresh)	15		ns	
Ct 705	tWRP	WE# Hold from RAS# Active (DRAM Refresh)	15		ns	
Ct 706	tRDS	RAS# Active Delay from SYSCLK (DRAM DMA/Master)		55	ns	
Ct 707	tADS	Address Valid Delay from SYSCLK (DRAM DMA/Master)		65	ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It1		SYSCLK Period	125		ns	
It2		SYSCLK Low Time @V_{IL} = 1.5V	50		ns	
It3		SYSCLK High Time @V_{IL} = 1.5V	50		ns	
It4		SYSCLK Rise Time and Fall time		10	ns	
It5		RESETDRV Inactive (LOW) from PWRGOOD Active (HIGH)		40	ns	
It5a		RESETDRV Active (HIGH) from SYSCLK (During Resume after Suspend)		125		
It6a		A20GATE Active (HIGH) Delay from KBDA20 Active (HIGH)		30	ns	
It6b		A20GATE Active (HIGH) Delay from SYSCLK *		45	ns	
It7		SYSCLK to KBDCLK Delay		30	ns	
It8a		RC#/PERR#/IOCHCK# Pulse Width	250		ns	
It8b		RC#/PERR#/IOCHCK# Setup to SYSCLK Falling Edge	12		ns	
It9a		CPURESET Active (HIGH) from SYSCLK	5	50	ns	
It10a		NMI Active (HIGH) from SYSCLK		125	ns	
It10b		NMI Inactive from IOW# Active (LOW)	0			
It11		RTCRESET# Pulse Width	5		ns	
It14		BALE hold from SYSCLK	2	45	ns	
It15		IOR#/IOW#/INTA# Input Active (LOW) Delay from SYSCLK Low		20	ns	
It15a		IOR#/IOW#/MEMW# Output Active (LOW) Delay from SYSCLK		90	ns	
It16		IOR#/IOW#/INTA#/MEMW#/MEMR# Input Inactive from SYSCLK		35	ns	
It16a		IOR#/IOW# Output Inactive from SYSCLK		120	ns	
It17		ZEROWS# Output Active from SYSCLK		65	ns	
It18		ZEROWS# Output Inactive from SYSCLK	0		ns	
It19		BALE Setup to SYSCLK (DMA Cycle)	18		ns	
It20		IOCHRDY Input Active Setup to SYSCLK	15		ns	
It20a		IOCHRDY Input Inactive Setup to SYSCLK	15		ns	
It21		DMA8/16# Active Delay from SYSCLK		65	ns	
It22		DMA8/16# Inactive Delay from SYSCLK (4 MHz DMACLK)		65	ns	
It22a		DMA8/16# Inactive Delay from SYSCLK Low (8 MHz DMACLK)		65	ns	
It23		AEN Active from HLDA Active		35	ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It24		AEN Inactive Delay from HLDA Inactive		35	ns	
It24f		AEN Inactive from SYSCLK		65	ns	
It25		SA15:0, SBHE# Valid Delay from SYSCLK	10	100	ns	
It26		SA16 (Only if DMA8/16# = 0) SA15:0, SHBE# Valid Output Hold from SYSCLK	6		ns	
It26a		SA16 (Only if DMA 8/16# = 1), LA17:23 Valid Output Hold from IOR#/IOW#/MEMR#/MEMW# Output	10		ns	
It26f		SA16:0, LA17:23, SBHE# Float Delay from SYSCLK		90	ns	
It27		DACKx# Active Delay from SYSCLK (4 MHz DMACLK)		75	ns	
It27a		DACKx# Active Delay from SYSCLK Low (8 MHz DMACLK)		75	ns	
It28		DACKx# Inactive Delay from SYSCLK (4 MHz DMACLK)		75	ns	
It28a		DACKx# Inactive Delay from SYSCLK Low (8 MHz DMACLK)		75	ns	
It29		IOR#/IOW#/MEMW# Float-to-Drive-Inactive from SYSCLK		75	ns	
It30		IOR#/IOW#/MEMW# Float Delay from SYSCLK#		75	ns	
It30a		SMRAMCS# Setup to MEMR#/MEMW# Active		75	ns	
It31		MEMR#/MEMW# Input Active Delay from SYSCLK		70	ns	
It31a		MEMR#/MEMW# Output Active Delay from SYSCLK		70	ns	
It32a		MEMR#/MEMW# Output Inactive Delay from SYSCLK		75	ns	
It33		T/C Active Delay from SYSCLK		85	ns	
It34		T/C Inactive Delay from SYSCLK		85	ns	
It35		TIM2CLK2 Period	125		ns	
It36		TIM2CLK2 Low Time	55		ns	
It37		TIM2CLK2 High Time	55		ns	
It38		TIM2CLK2 Rise Time		25	ns	
It39		TIM2CLK2 Fall Time		25	ns	
It40		TIM2GAT2 High Pulse Width	45		ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It41		TIM2GAT2 Low Pulse Width	45		ns	
It42		TIM2GAT2 Setup to TIM2CLK2	45		ns	
It43		TIM2GAT2 Hold from TIM2CLK2	45		ns	
It44		TIM2OUT2 from TIM2CLK2 High to Low		110	ns	
It45		TIM2OUT2 from TIM2GAT2 High to Low		110	ns	
It46		SPKR Active Delay from TIM2GAT2 (When EXTAUD is Set)		120	ns	
It50		REFRESH# Active to MEMR# Output Active	150		ns	
It52		Address Valid to MEMR# Active	40		ns	
It53		MEMR# Output Inactive from IOCHRDY Input Low to High (During a Master Refresh)	125		ns	
It55		IOCHRDY Pulse Width		750	ns	
It56		MEMR# Output Pulse Width for Refresh			SYSCLK	
It59		FLPCS#/C8042CS#/HDCS0#/HDCS1# Active Setup to Command Active	25		ns	
It60		FLPCS#/C8042CS#/HDCS0#/HDCS1# Output Hold from Command Inactive	10		ns	
It60a		PMRAMCS# Hold from MEMR#/MEMW#	10		ns	
It69		DRQx Setup to SYSCLK High to Low	0		ns	
It79		EXTRTCAS Pulse Width	3	4	SYSCLK	
It80		IOCS16# Setup to Command	10		ns	
It81		IOCS16# Hold from Command	10		ns	
It82		STPCLK# Delay from SYSCLK		100	ns	
It83		PMI# from SYSCLK		100	ns	
It84		SMOUT from SYSCLK		100	ns	
It85		SUS_STAT# from SYSCLK		100	ns	
It86		IOCHRDY Output from SYSCLK		60	ns	
It94		Delay from IOW# to Modem Output (RTS#, DTR#)		200	ns	
It109		KBDCLK Period (8 MHz)	125		ns	
		KBDCLK Period (4 MHz)	250		ns	
		KBDCLK Period (2 MHz)	500		ns	
It110		KBDCLK High Time (8 MHz)	40		ns	
		KBDCLK High Time (4 MHz)	95		ns	
		KBDCLK High Time (2 MHz)	200		ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It111		KBDCLK Low Time (8 MHz)	40		ns	
		KBDCLK Low Time (4 MHz)	95		ns	
		KBDCLK Low Time (2 MHz)	200		ns	
It117		HRQ Inactive to HLDA Inactive	185		ns	
It118		HLDA Inactive to HRQ Active (Back to Back Hold Acknowledge Cycles)	0		ns	
It120		IRQ1, 6, 10, 11: 12, 14, 15, ERROR# Pulse Width	50		ns	
It121		INTR Output Delay from IRQ1, 6, 10: 11, 12, 14, 15, ERROR#		100	ns	
It122		Data Output Valid from INTA# Active		120	ns	
It123		Data Output Hold from INTA# Inactive	10		ns	
It123f		Data Float from INTA# Inactive		35	ns	
It124a		SD7 Read Data Output Hold from MEMR# Inactive	5		ns	
It124f		SD7 Float from MEMR# Inactive		35	ns	
It125		Write Data Input Setup to MEMW#	40		ns	
It125a		XD7 Output Valid from MEMW# Active		45	ns	
It126		Write Data Input Hold from MEMW#	15		ns	
It126a		XD7 Output Hold from MEMW# Inactive	5		ns	
It126f		XD7 Float from MEMW# Inactive		45	ns	
It129		SMEMR#/SMEMW# Active from MEMR#/MEMW#		30	ns	
It129a		SMEMR#/SMEMW# Inactive from MEMR#/MEMW# Inactive	3	30	ns	
It200		BALE Active from SYSCLK Low	2	45	ns	
It201		Write Data Input Setup to IOW# Active	40		ns	
It202		Write Data Input Hold from IOW# Inactive	15		ns	
It203		Read Data Output Setup to IOR# Inactive	62		ns	
It204		Read Data Output Hold from IOR# Inactive	0		ns	
It204f		Data Bus Float from IOR#/MEMR#		35	ns	
It205		BALE Active Pulse Width	50		ns	
It206		Address Input Valid Setup to BALE Inactive	30		ns	
It207		AEN Active from SYSCLK during Indexed I/O Writes		80	ns	
It209		IOW# to EXTRTCAS		100	ns	
It210		XD7 Output Valid from IOW# Active		45	ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It211		XD7 Output Hold from IOW# Inactive	5		ns	
It211f		XD7 Output Float from IOW# Inactive		45	ns	
It212		EXTRTCRW#/EXTRTCDS Active from Command Active		35	ns	
It213		EXTRTCRW#/ EXTRTCDS Hold from Command Inactive		35	ns	
It214		XDEN# Output Delay from IOR#/IOW#, MEMR# Inputs *	10	50	ns	
It214a		XDEN# Output Delay from DACK2 Output		50	ns	
It215a		XDEN# Output Active from XDIR Output Active	0		ns	
It215b		XDIR Output Inactive from XDEN# Output Inactive	10		ns	
It216		SD7 Read Data Output Delay from XD7/HD7 Input		35	ns	
It217		SD7 Read Data Output Hold from IOR# Inactive	5		ns	
It217f		SD7 Float from IOR# Inactive		35	ns	
It218		Address-in Hold from Command Inactive	11		ns	
It219		HDENL#/HDENH# Output Active Delay from Command		35	ns	
It219a		HDENL#/HDENH# Output Inactive Delay from Command Inactive	5		ns	
It220	*	HD7 Output Valid from IOW# Active		45	ns	
It221		HD7 Output Hold from IOW# Inactive	10		ns	
It221f		HD7 Output Float from IOW# Inactive		35	ns	
It222		HALT# Input Setup to SYSCLK Low	20		ns	
It223		HALT# Input Hold from SYSCLK	20			
It224		XD7/HD7 Input Setup to IOR#/MEMR#	60		ns	
It225		XD7/HD7 Input Hold from IOR#/MEMR#	0		ns	
It230		XD7 Output Valid from EXTRTCRW# Active		35	ns	
It231		XD7 Output Hold from EXTRTCRW# Inactive	0		ns	
It231f		XD7 Output Float from EXTRTCRW#		35	ns	

6.0 SL SuperSet TIMING SPECIFICATIONS (Continued)

82360SL I/O Timing Specifications Summary (Continued)

Symbol	Alt Symbol	Parameter	Min	Max	Unit	Notes
It305		SA16, LA23:17 Valid Delay from SYSCLK	10	150	ns	
It311		HRQ Output Active from SYSCLK		45	ns	
It312		HLDA Setup to SYSCLK	18		ns	
It314		HRQ Inactive from SYSCLK	5		ns	
It317		REFREQ Active from SYSCLK		45	ns	
It319		REFREQ Inactive from SYSCLK		45	ns	
It322		MASTER# Active to REFRESH# Input Active Delay	25		ns	
It324		REFRESH# Output Active from HLDA		35	ns	
It325		REFRESH# Output Inactive from SYSCLK	5		ns	
It326		REFRESH# Input to REFREQ Active		30	ns	
It327		REFRESH# Input to REFREQ Inactive	5		ns	
It328		REFRESH# Pulse Width	4	5	SYSC	
It329		REFREQ Pulse Width during Master# Cycle	4	5	SYSC	
It330		DACKx# to MASTER# Delay	0		ns	
It331		AEN Delay from MASTER#	0	49	ns	
It332		Alternate Master Drives Address and Data		125	ns	
It333		MASTER# Delay from DRQx Inactive		100	ns	
It334		Alternate Master Tri-States Bus Signal	0		ns	

7.0 SL SuperSet TIMING DIAGRAMS

7.1 386™SL CPU Timing Diagrams

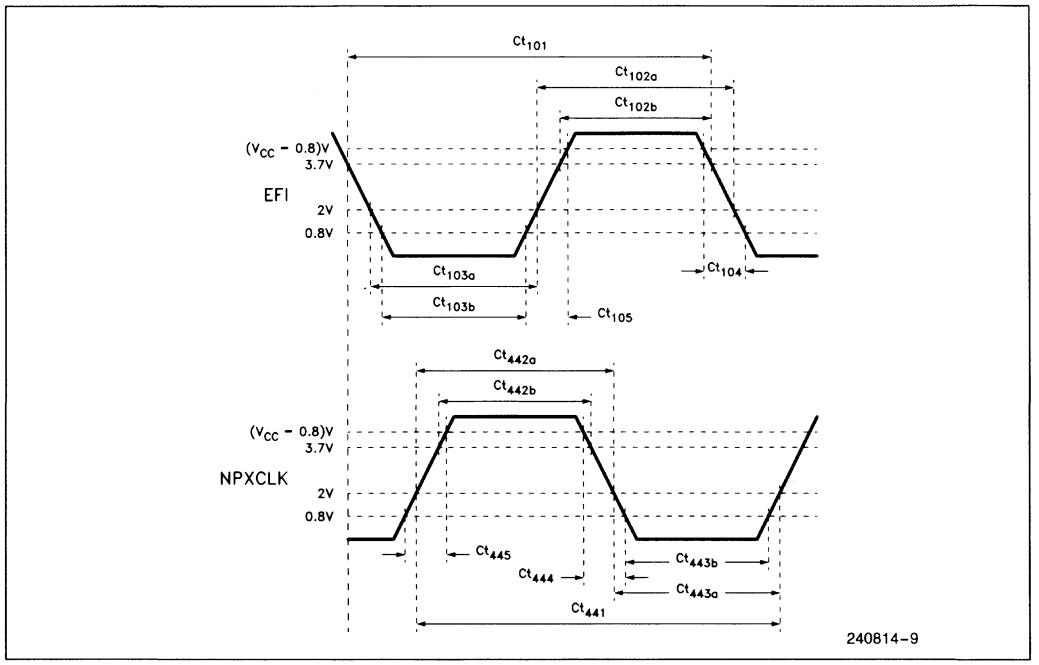


Figure 7.1.1. Clocks

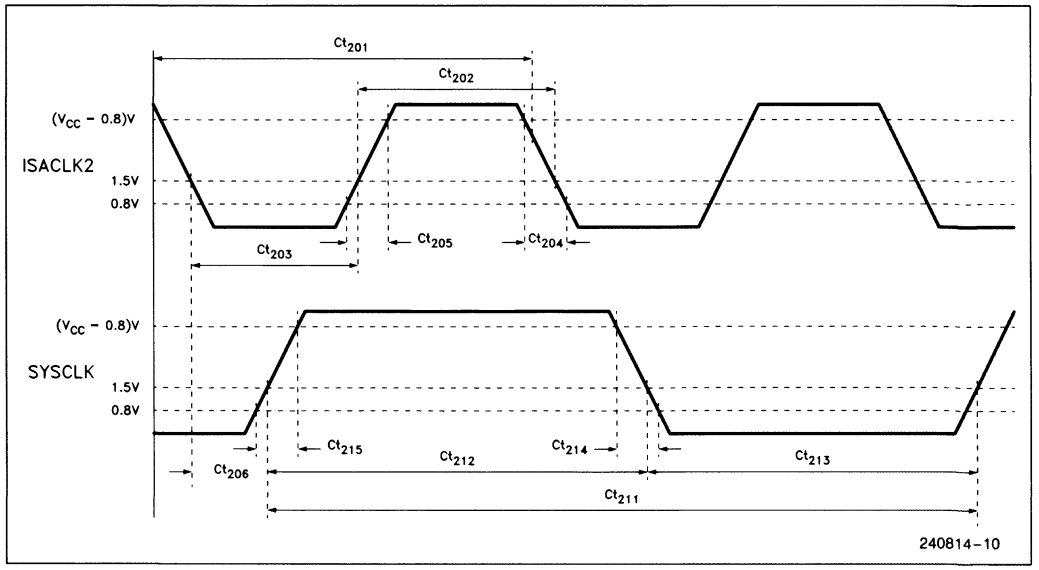


Figure 7.1.2. Clocks

7.1 386™SL CPU Timing Diagrams (Continued)

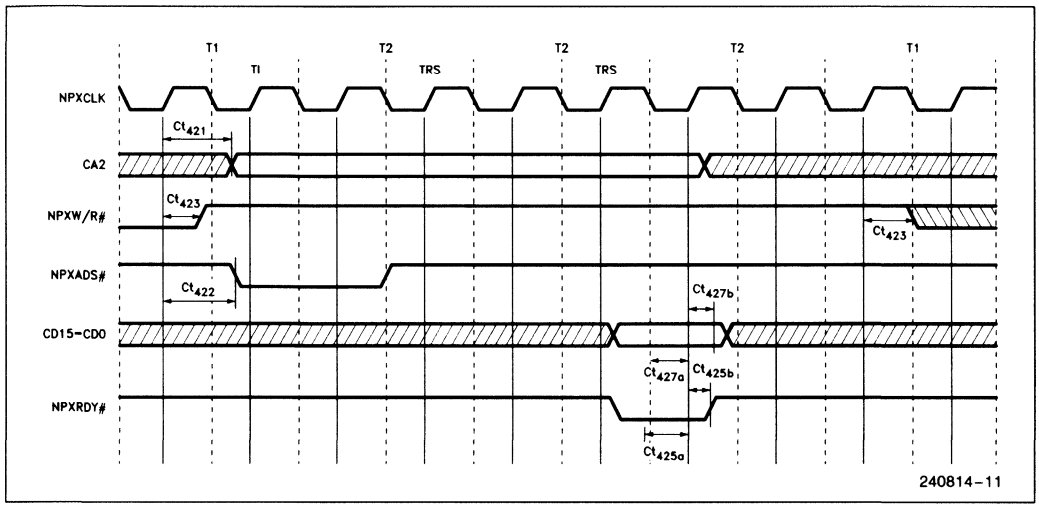


Figure 7.1.3. 386 SL CPU Read from MCP

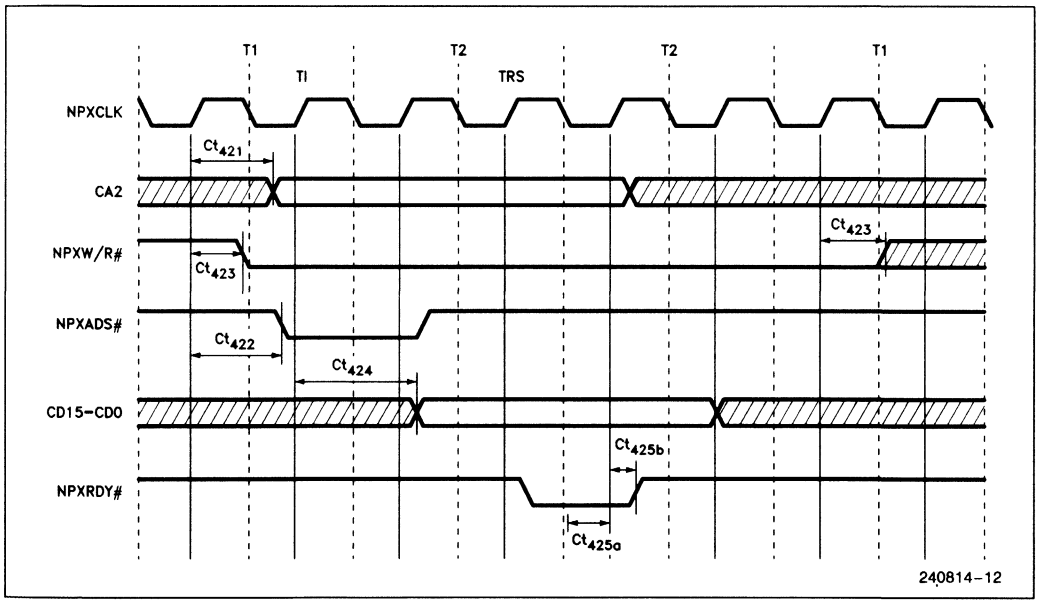
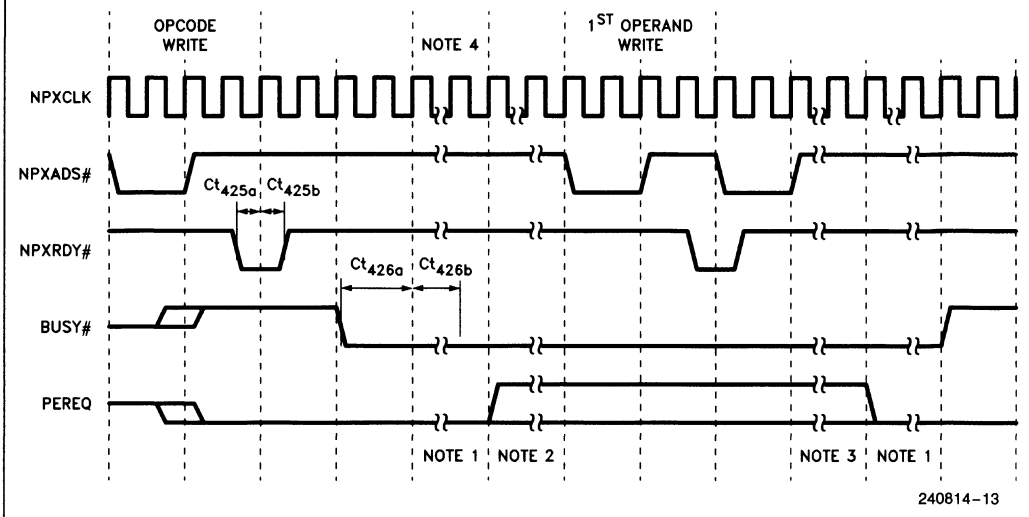


Figure 7.1.4. 386 SL CPU Write to MCP

7.1 386™SL CPU Timing Diagrams (Continued)



NOTES:
1. Instruction dependent.
2. PEREQ is an asynchronous input to the 386 SL CPU. Instruction dependent as to when it is asserted.
3. Additional operand transfers.
4. Memory read (operand) cycles not shown.

Figure 7.1.5. MCP BUSY# and PEREQ Timings

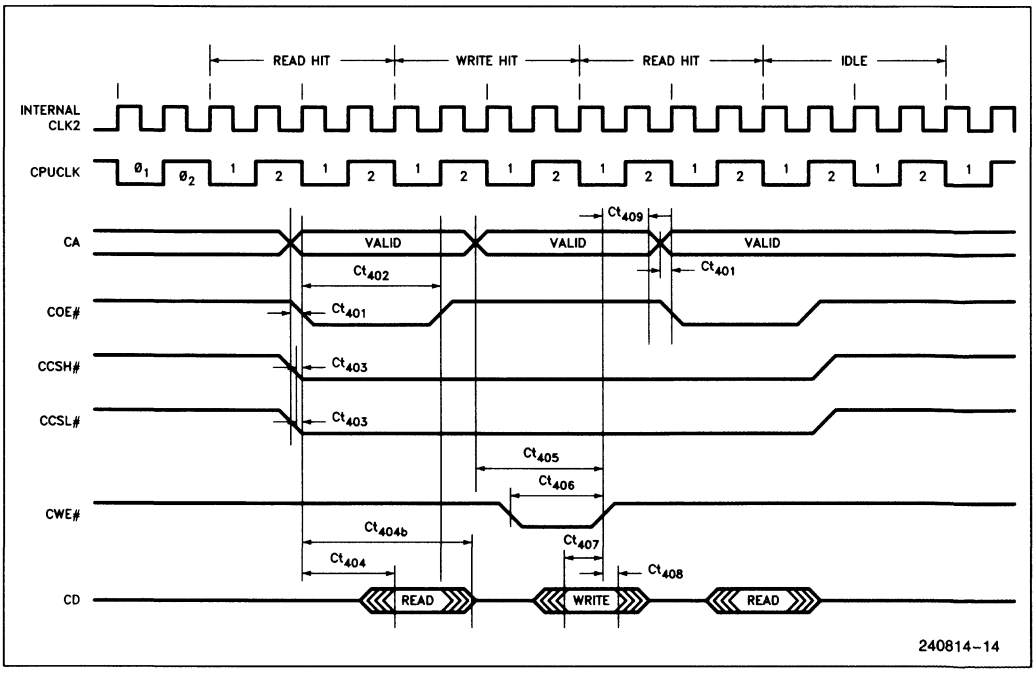


Figure 7.1.6. Cache Read/Write Hit Cycles

7.1 386™SL CPU Timing Diagrams (Continued)

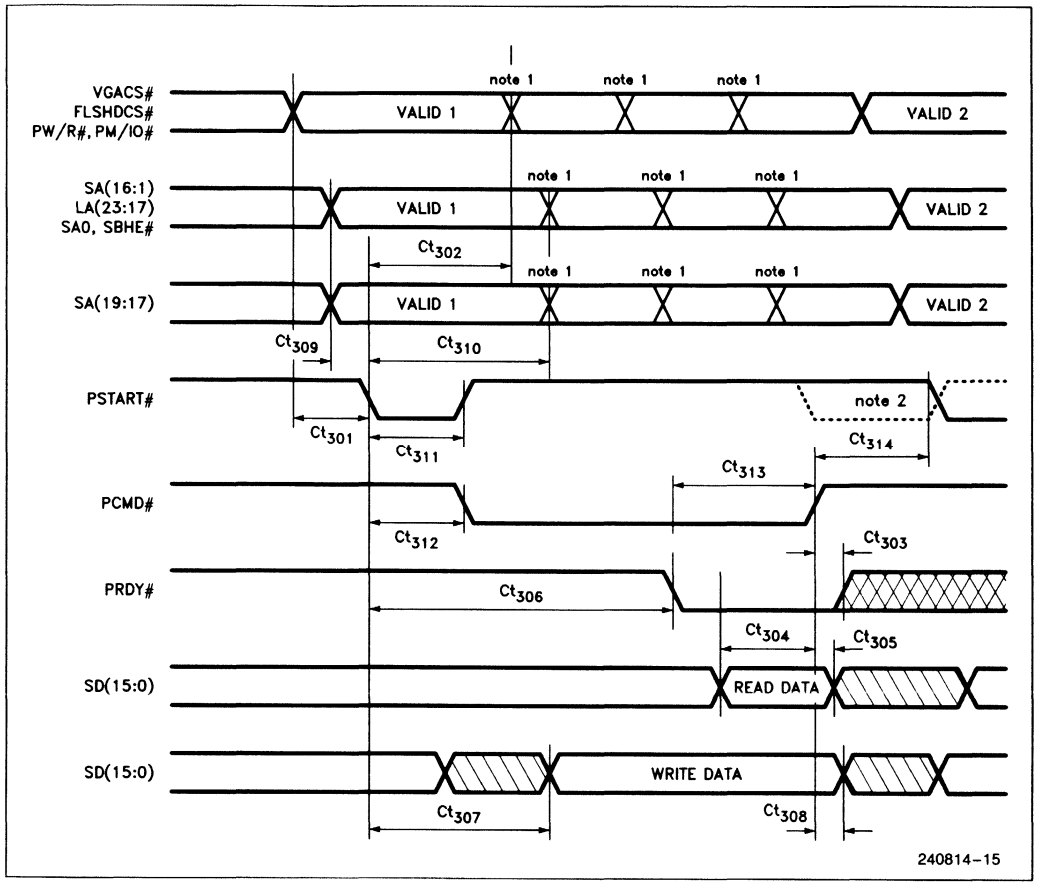


Figure 7.1.7. PI-Bus Timings

7.1 386™SL CPU Timing Diagrams (Continued)

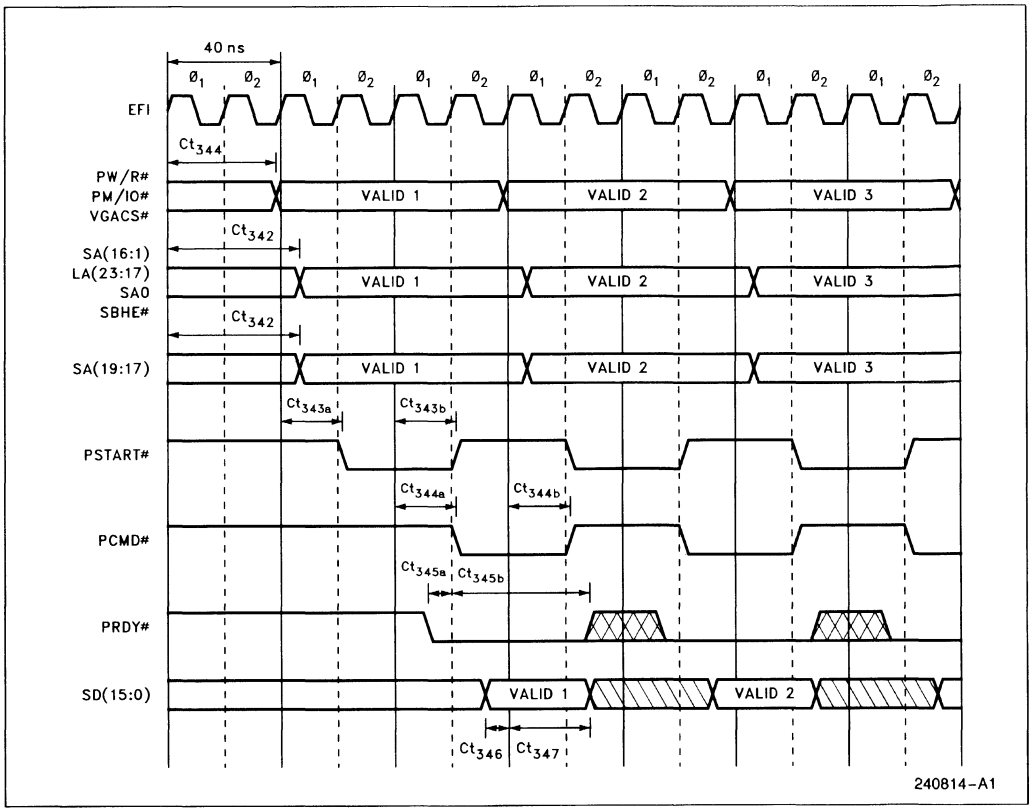


Figure 7.1.8a. PI Bus Synchronous CPU Generated Cycles (Read)

7.1 386™SL CPU Timing Diagrams (Continued)

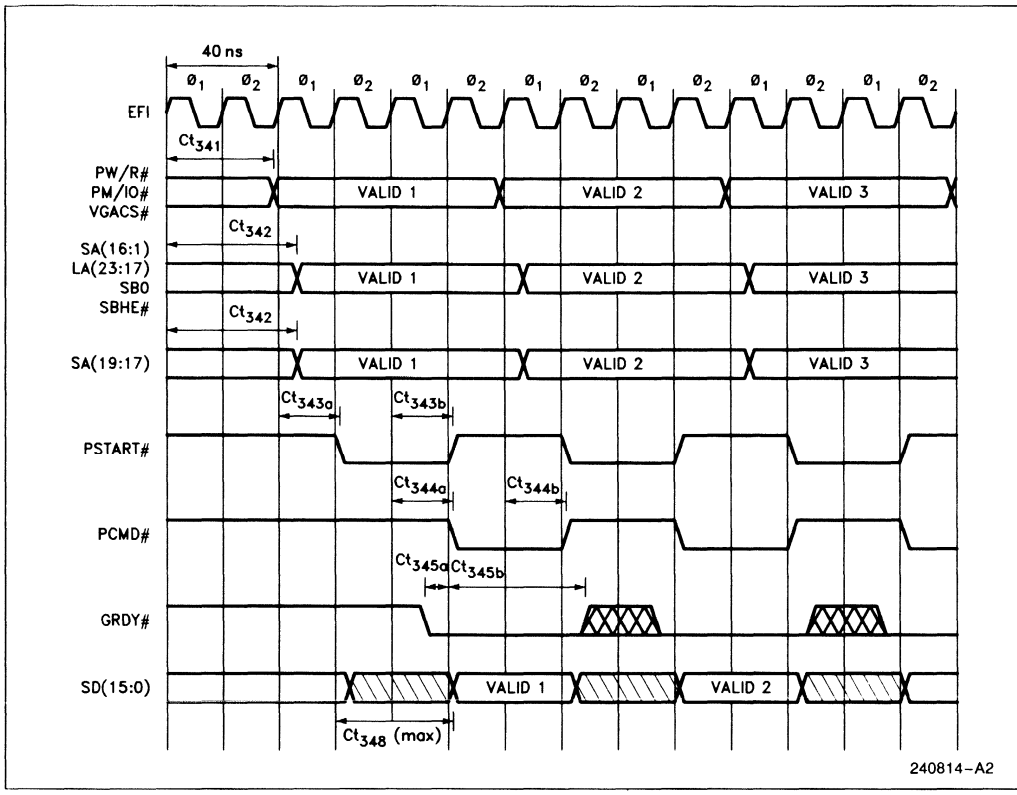


Figure 7.1.8b. PI-Bus Synchronous CPU Generated Cycles (Write)

7.1 386™SL CPU Timing Diagrams (Continued)

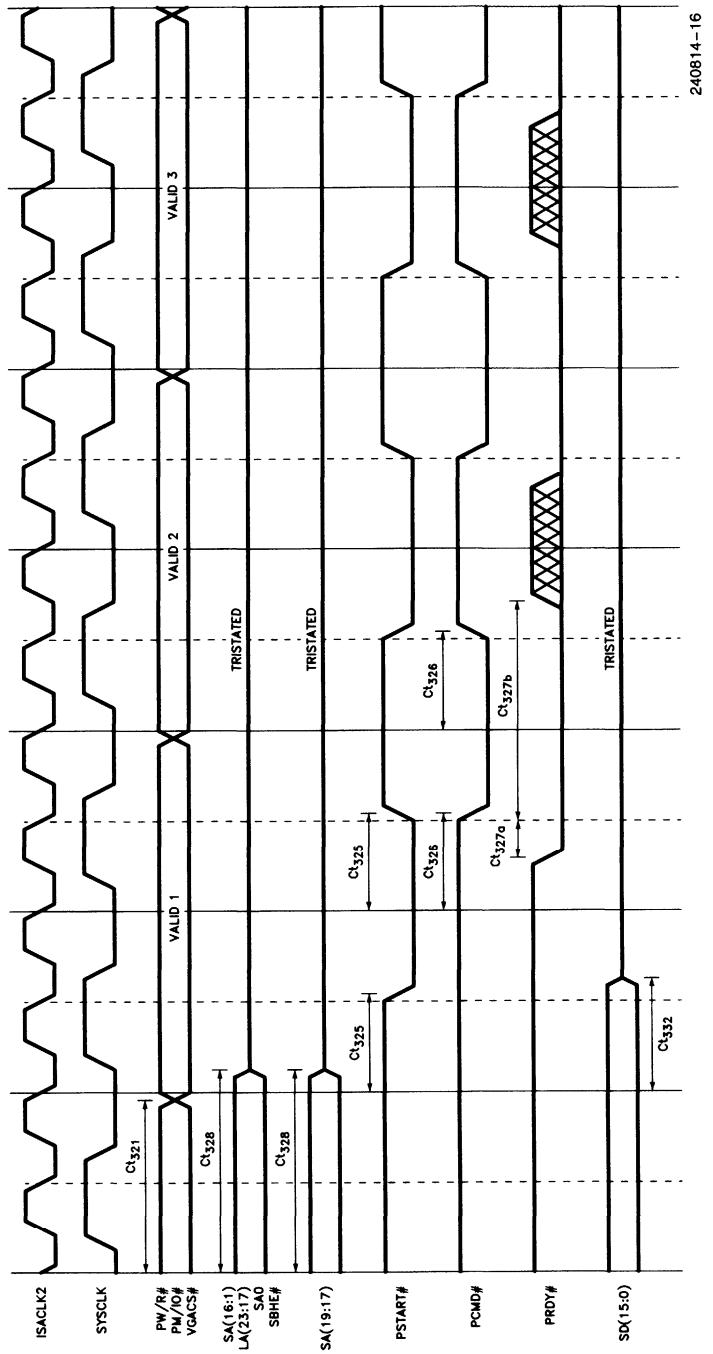


Figure 7.1.9. PI-Bus Slave Controller Generated Timings

7.1 386™SL CPU Timing Diagrams (Continued)

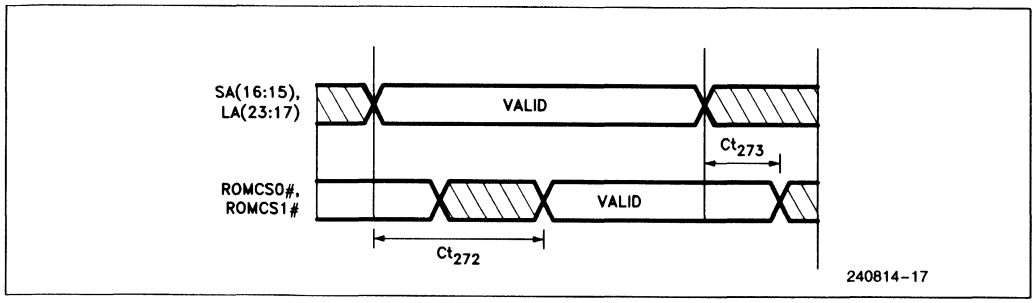


Figure 7.1.10. ISA Bus Slave Controller Generated Timings (ROMCS0#/CS1# with respect to Address)

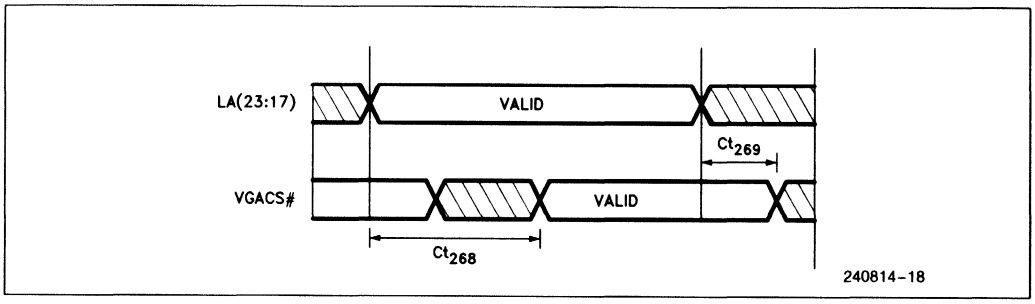


Figure 7.1.11. ISA Bus Master Controller Generated Timings (VGACS# with respect to Address)

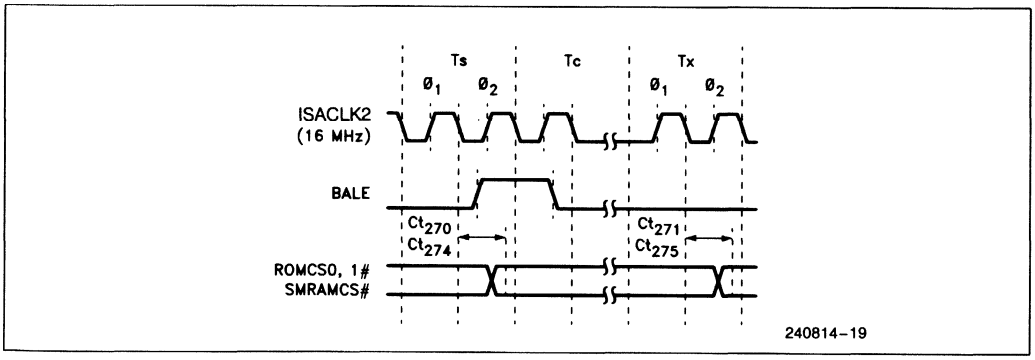


Figure 7.1.12. ROMCS0, ROMCS1, SMRAMCS# Propagation Delays

7.1 386™SL CPU Timing Diagrams (Continued)

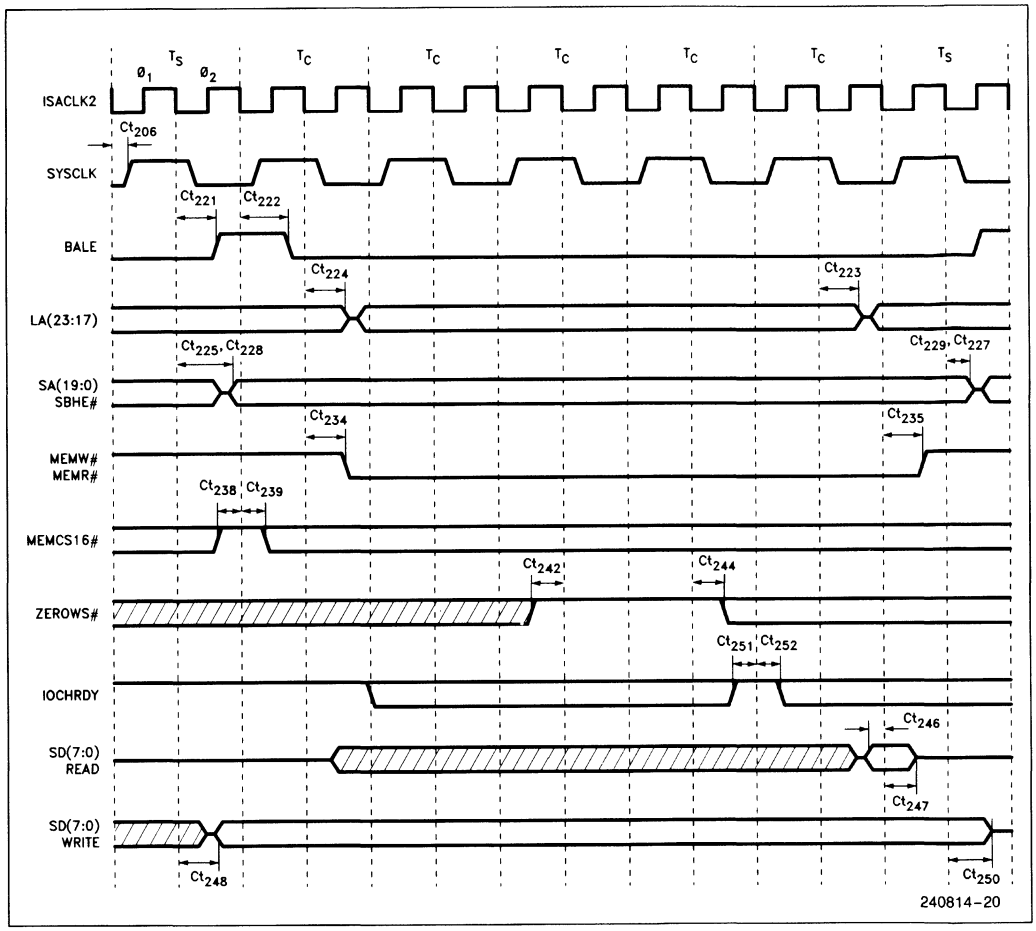


Figure 7.1.13. ISA Bus 8-Bit Memory Read/Write Standard ISA BUS Cycle (6 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

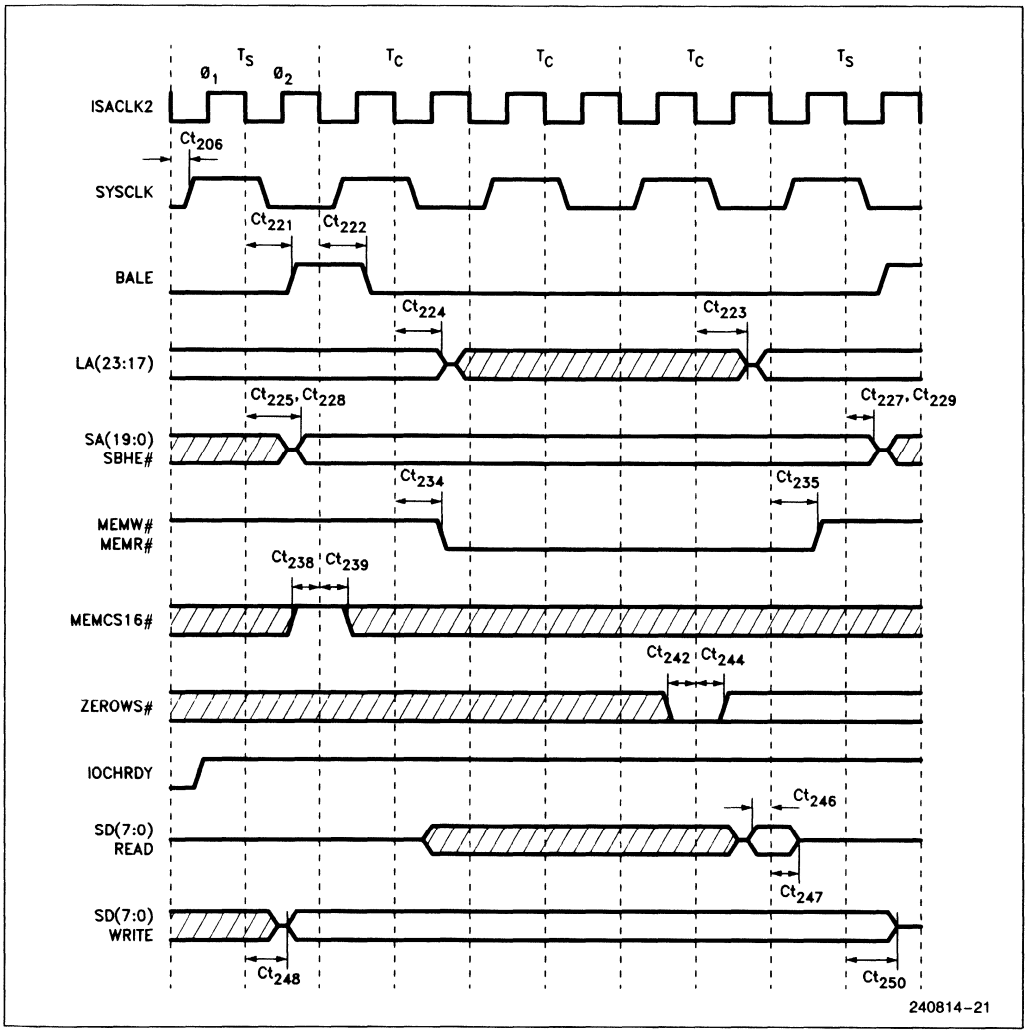


Figure 7.1.14. ISA Bus 8-Bit Memory Read/Write with ZEROWS# Asserted (3 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

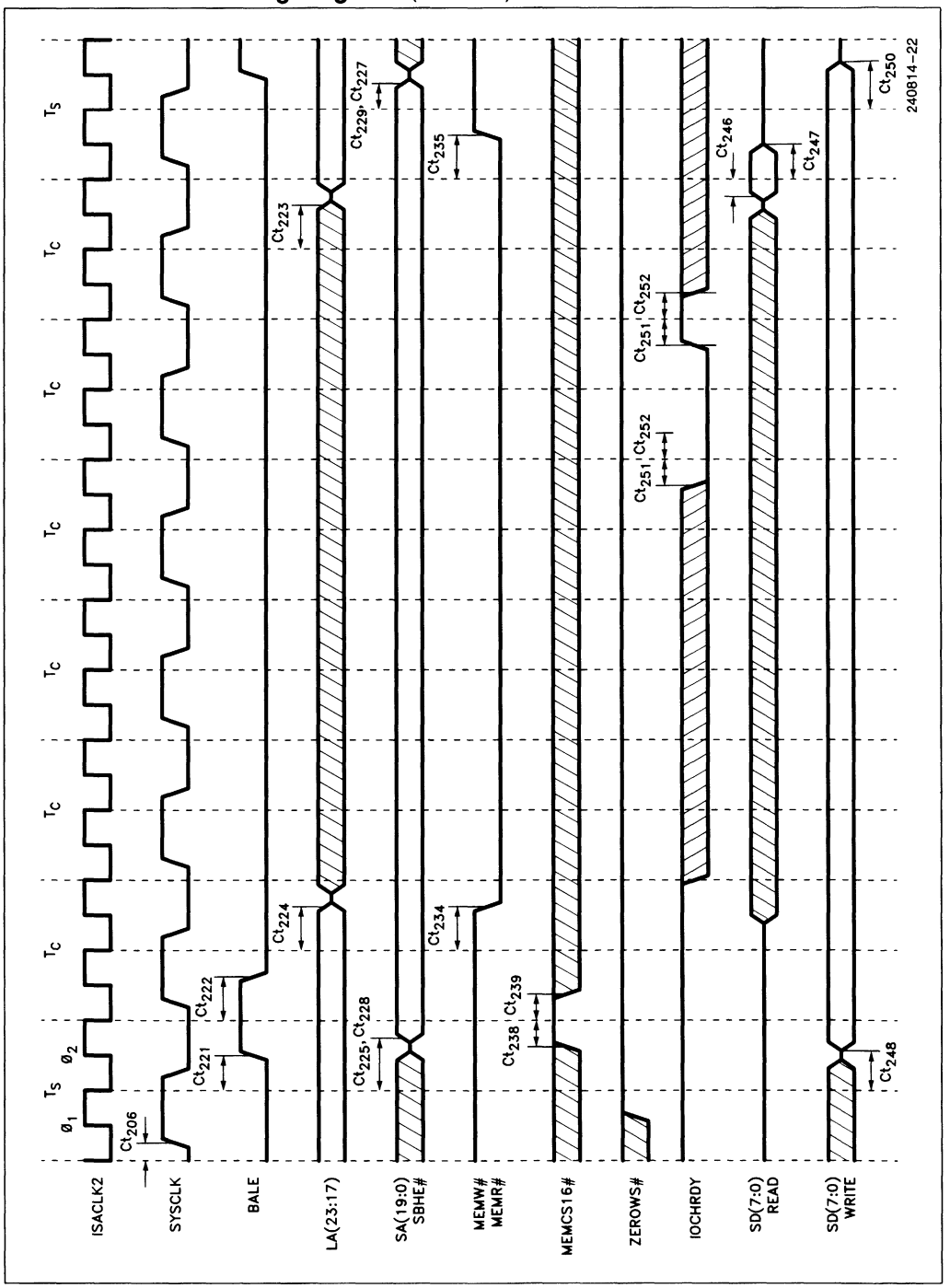


Figure 7.1.15. ISA Bus 8-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

7.1 386™SL CPU Timing Diagrams (Continued)

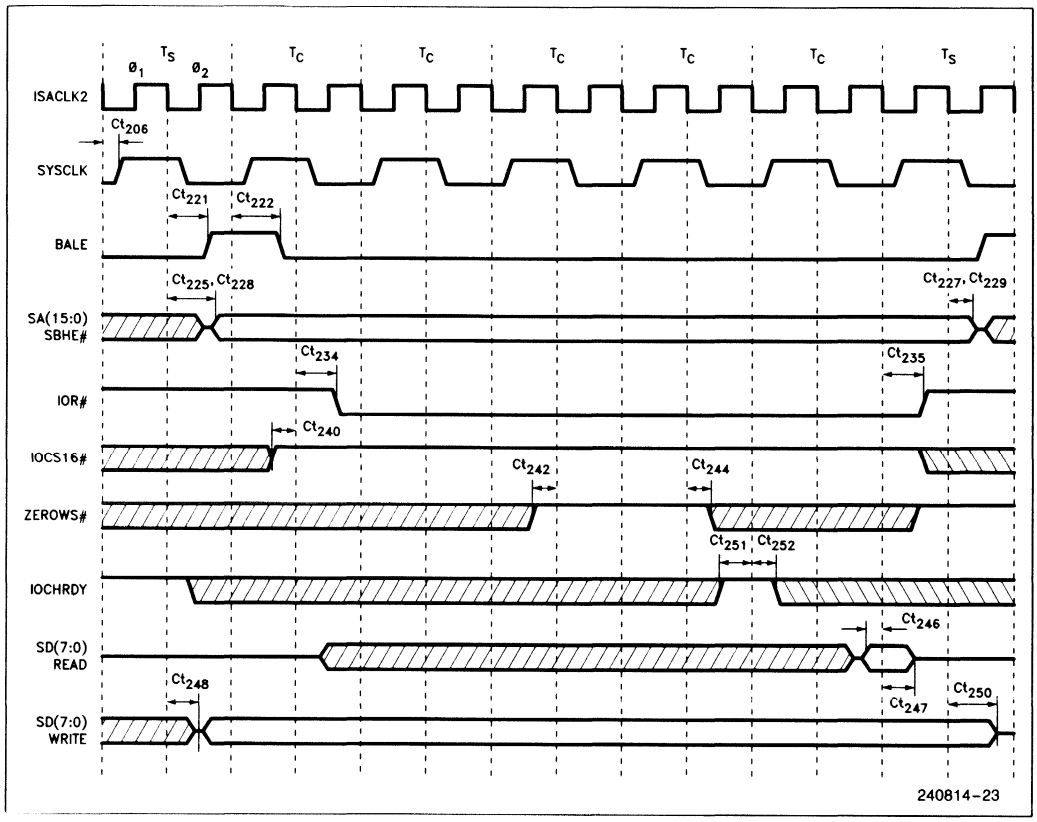


Figure 7.1.16. ISA Bus 8-Bit I/O Read/Write Standard ISA BUS Cycle (6 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

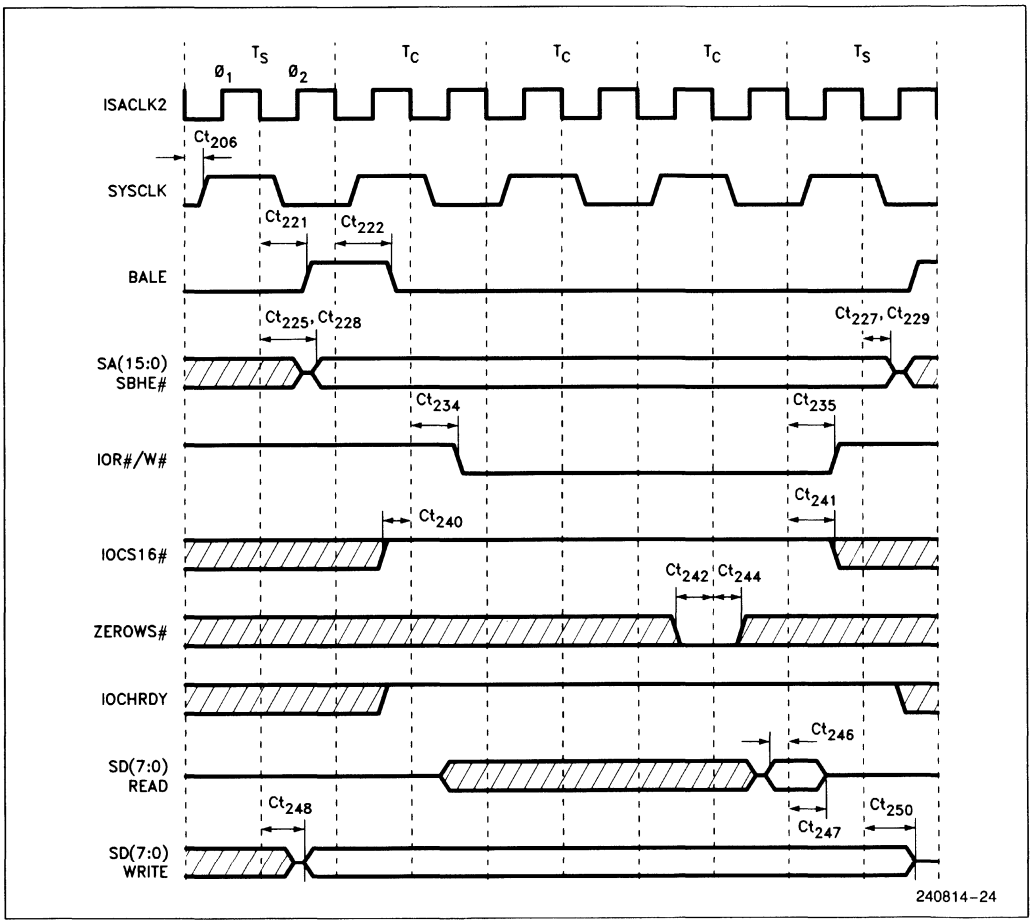


Figure 7.1.17. ISA Bus 8-Bit I/O Read/Write with ZEROWS# Asserted (3 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

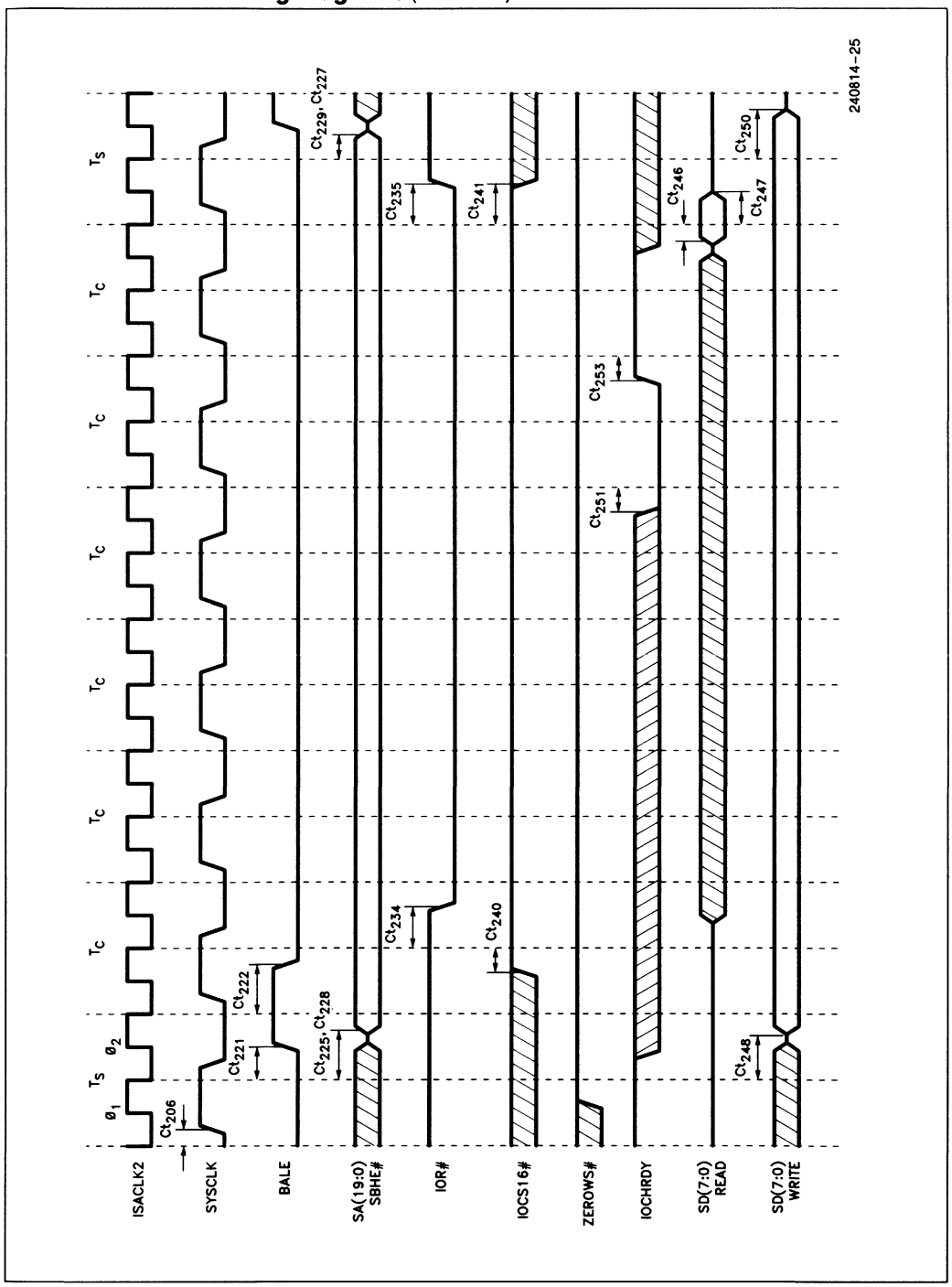


Figure 7.1.18. ISA Bus 8-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

7.1 386™SL CPU Timing Diagrams (Continued)

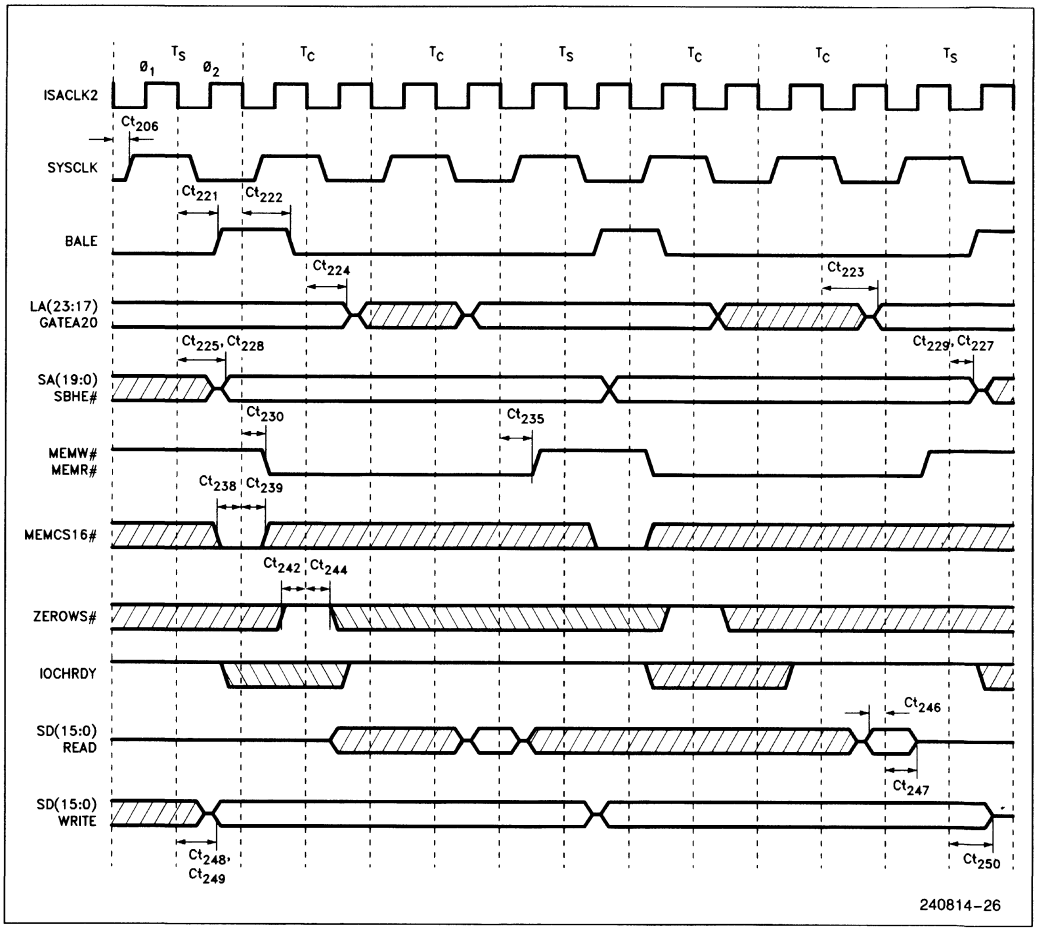


Figure 7.1.19. ISA Bus 16-Bit Memory Read/Write Standard ISA BUS Cycle (3 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

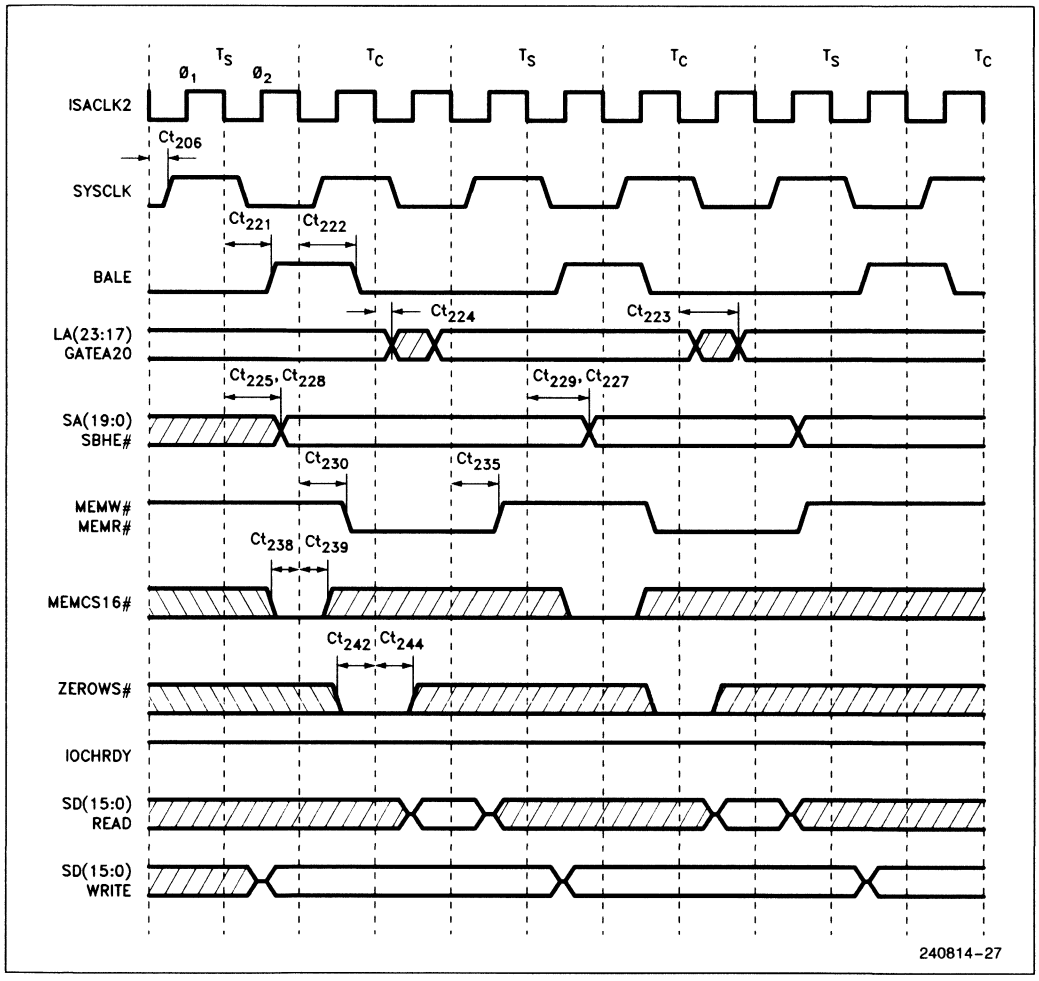


Figure 7.1.20. ISA Bus 16-Bit Memory Read/Write with ZEROWS# Asserted (2 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

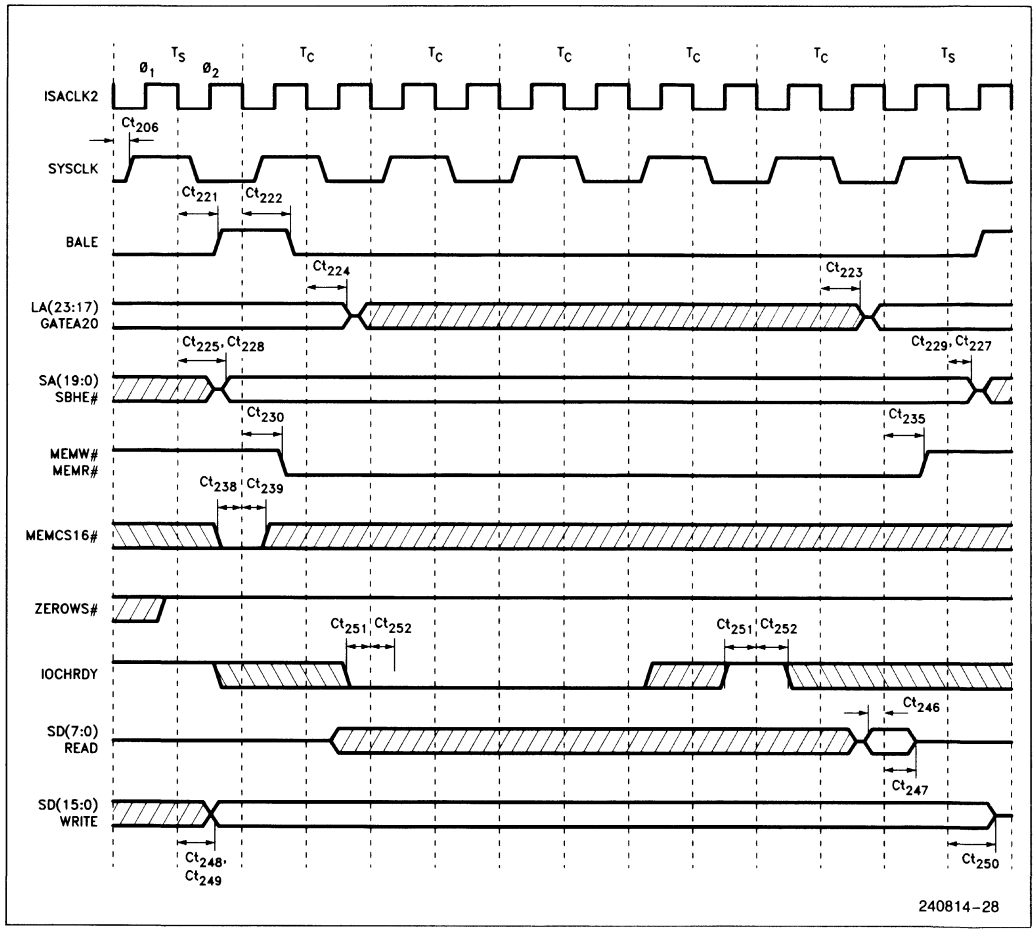


Figure 7.1.21. ISA Bus 16-Bit Memory Read/Write with IOCHRDY De-Asserted (Added Wait States)

7.1 386™SL CPU Timing Diagrams (Continued)

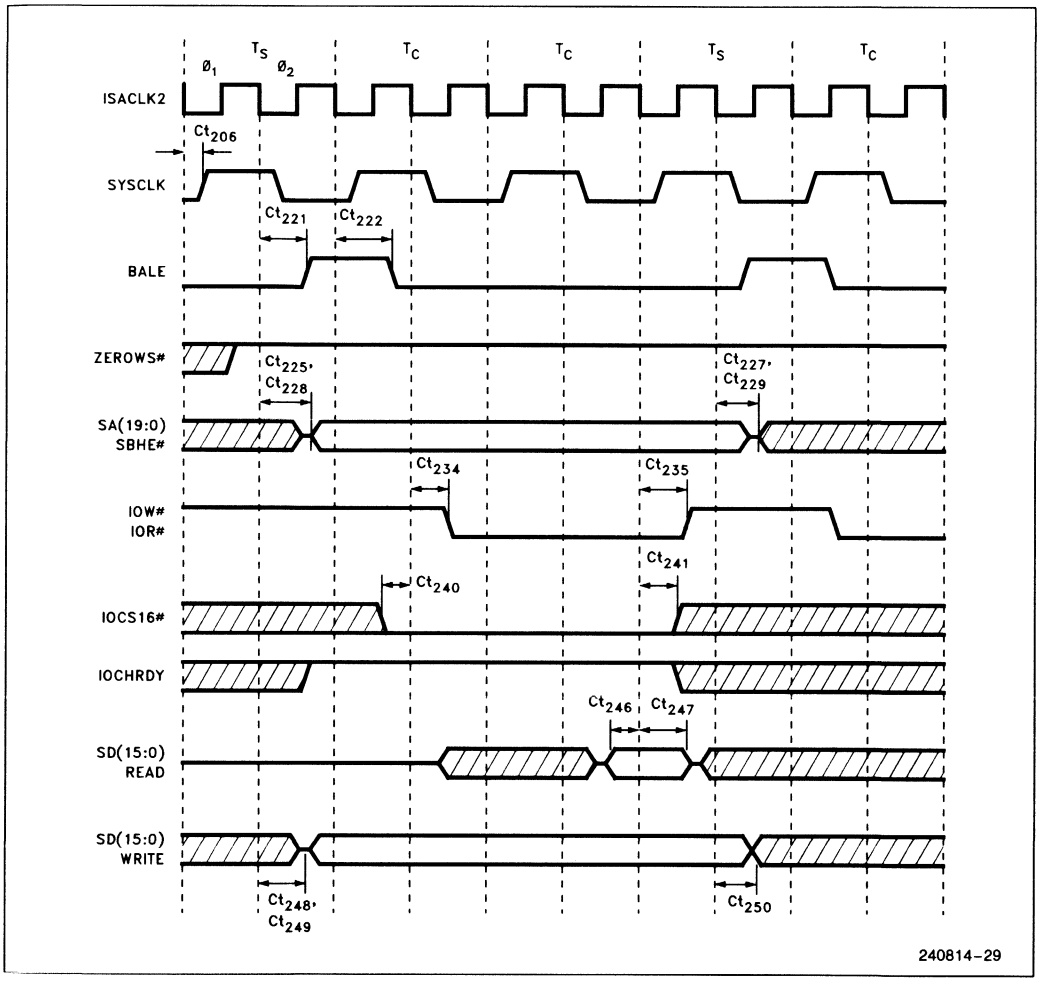


Figure 7.1.22. ISA Bus 16-Bit I/O Read/Write Standard ISA BUS Cycle (3 SYSCLKs)

7.1 386™SL CPU Timing Diagrams (Continued)

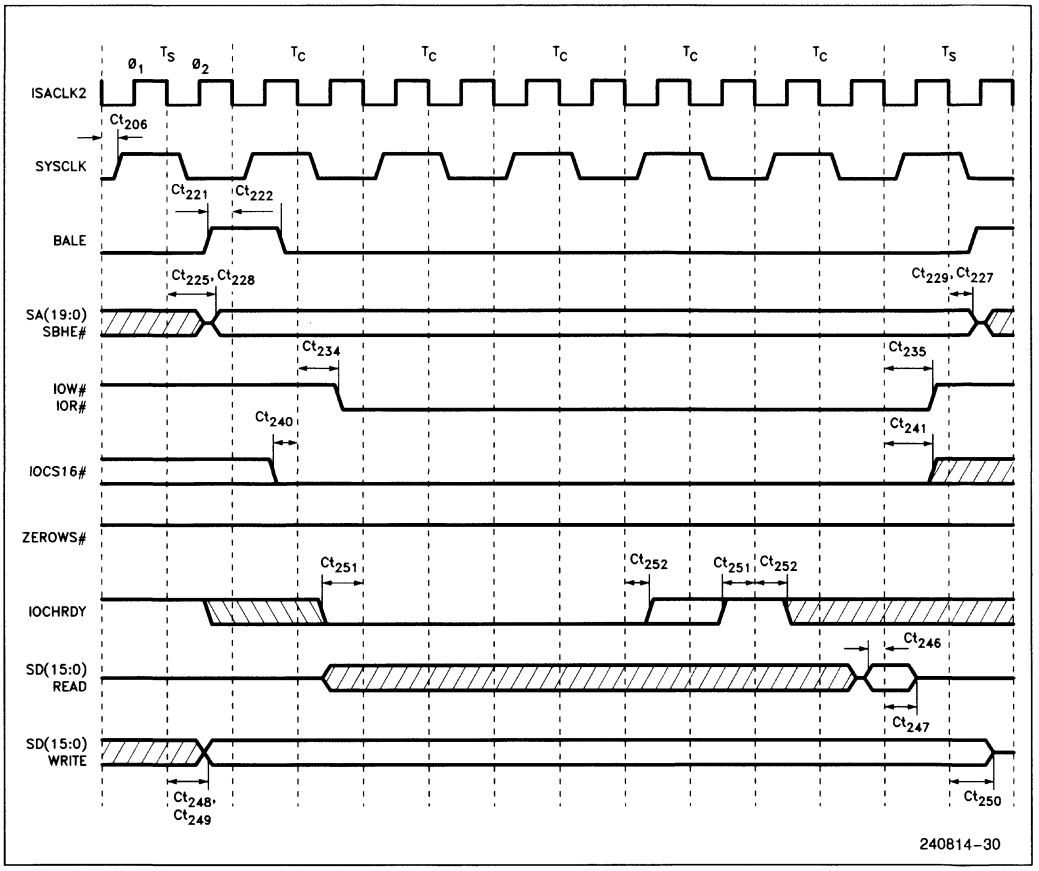


Figure 7.1.23. ISA Bus 16-Bit I/O Read/Write with IOCHRDY De-Asserted (Added Wait States)

7.1 386™SL CPU Timing Diagrams (Continued)

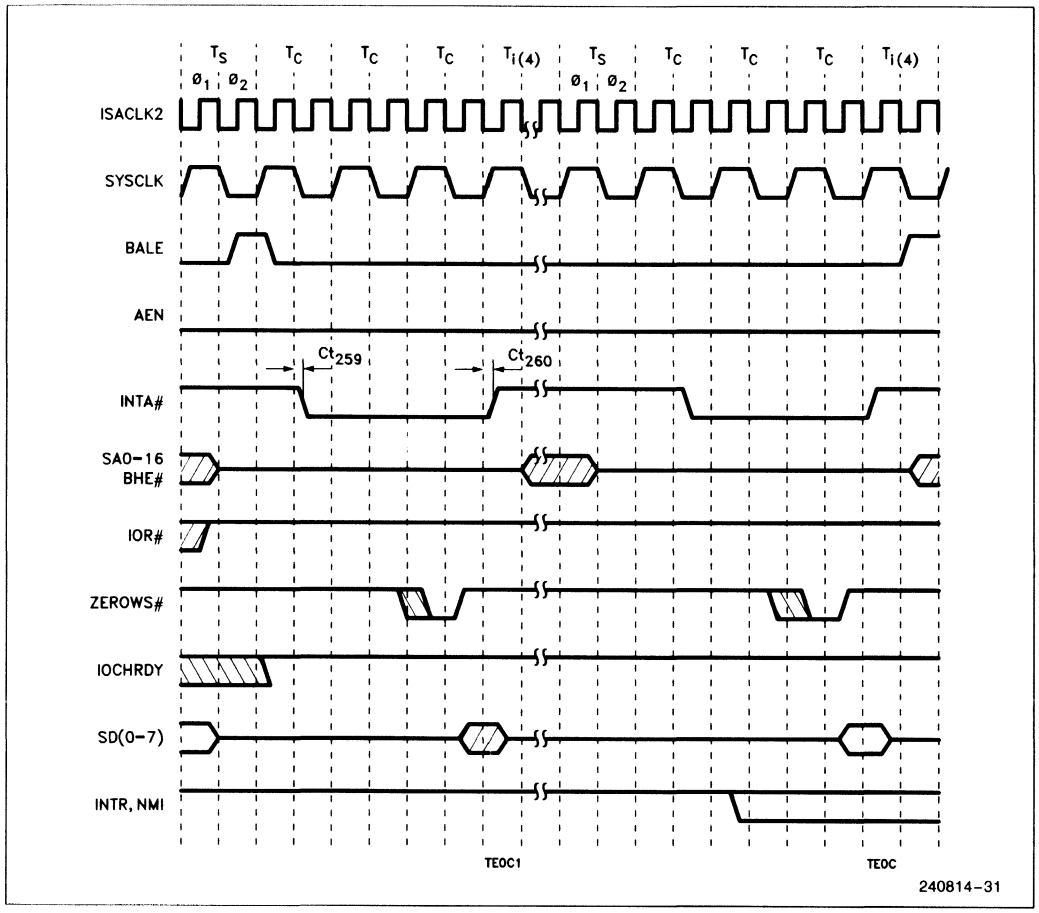


Figure 7.1.24. ISA Bus Interrupt Acknowledge Bus Cycle

7.1 386™SL CPU Timing Diagrams (Continued)

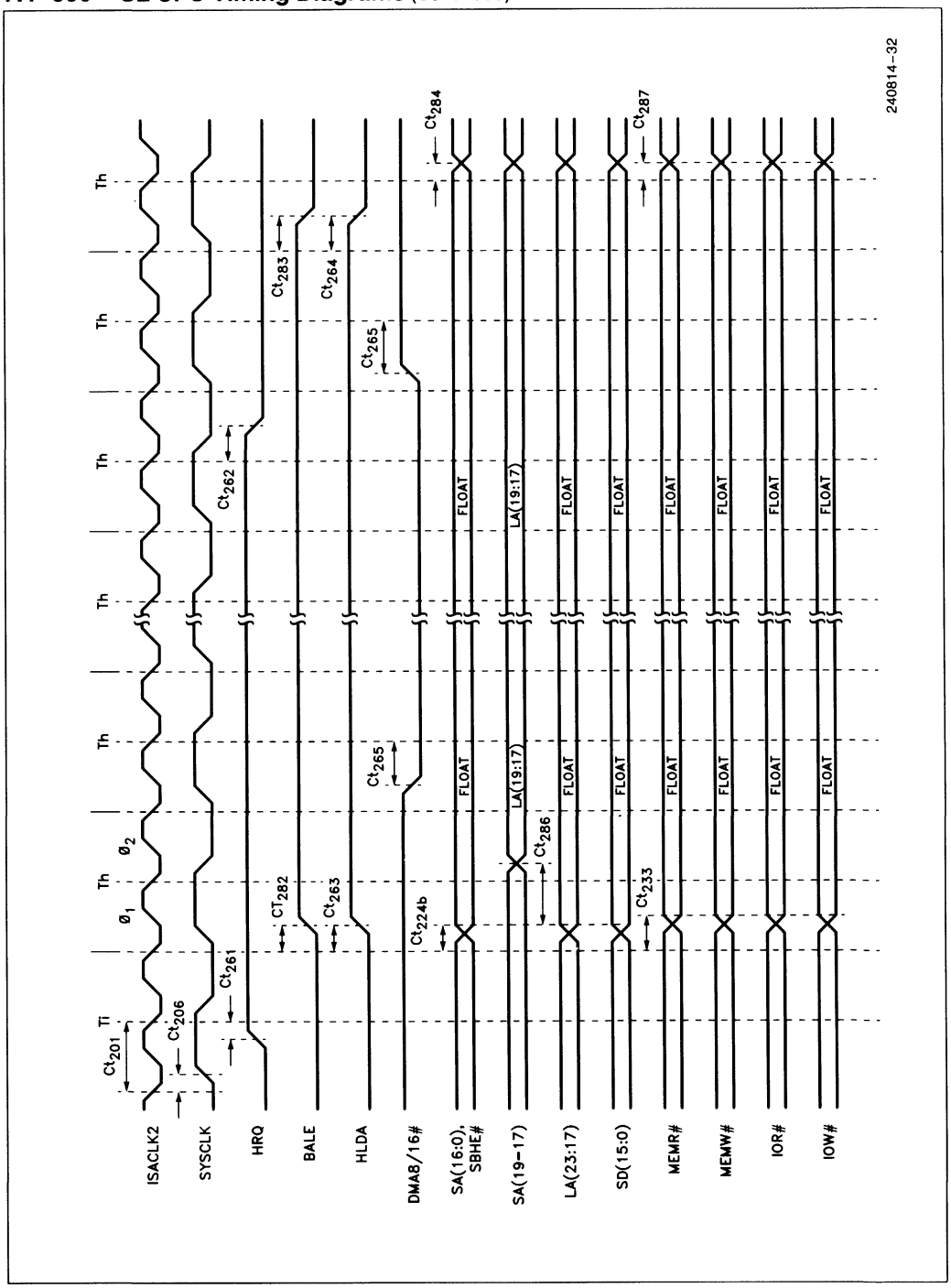


Figure 7.1.25. ISA Bus Controller DMA Cycle

7.1 386™SL CPU Timing Diagrams (Continued)

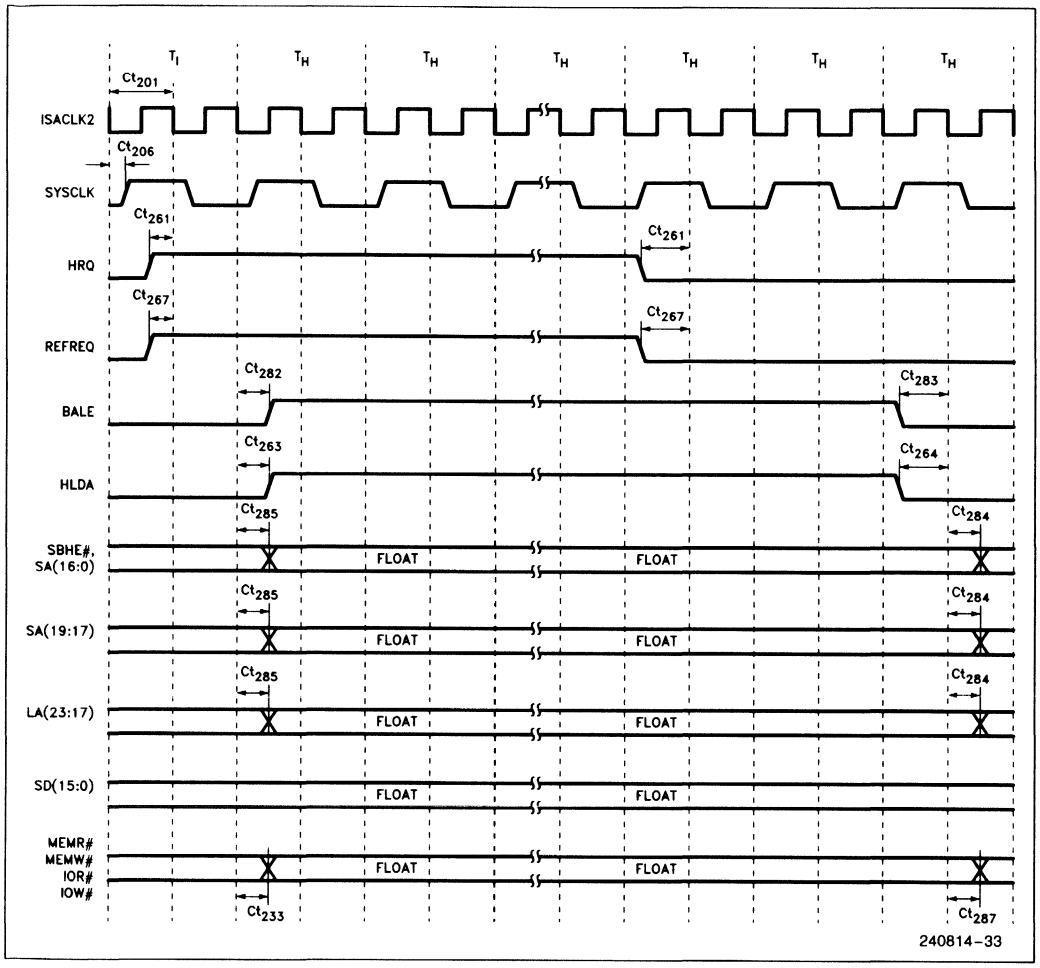
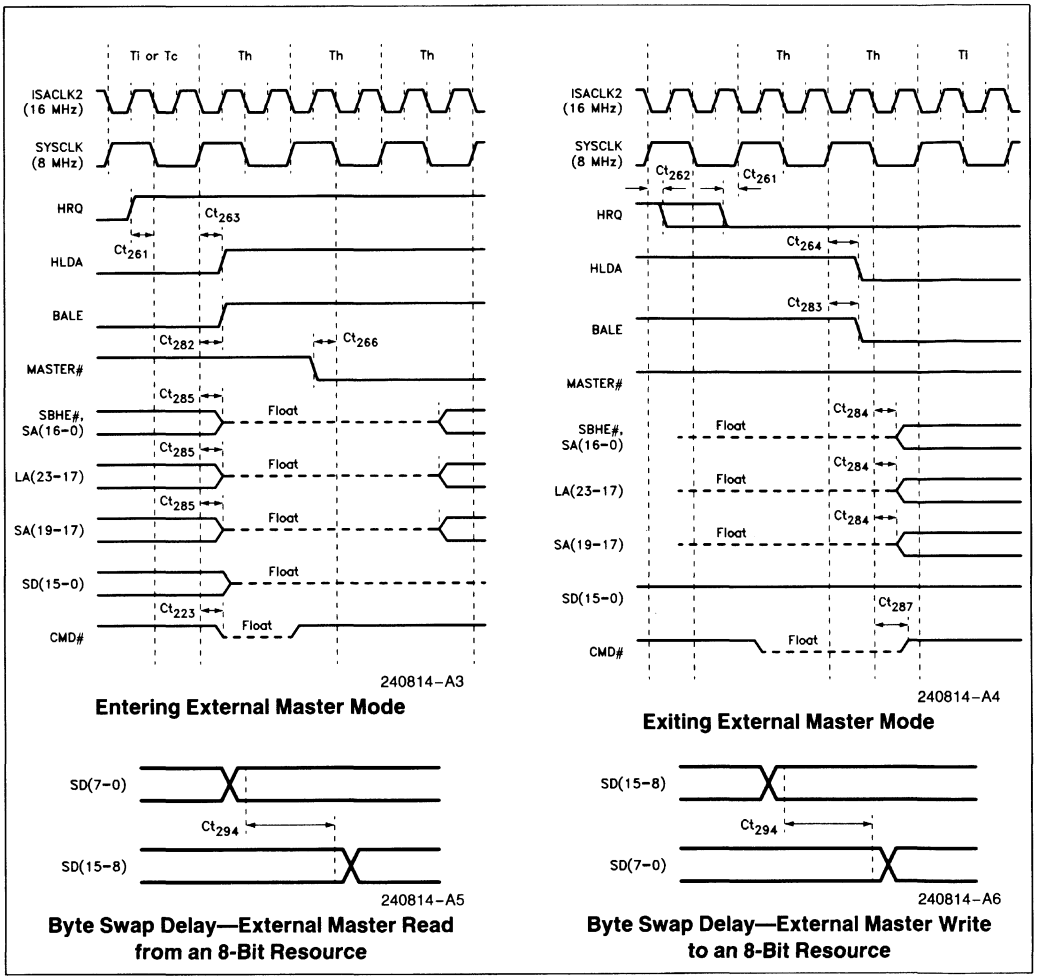


Figure 7.1.26. ISA Bus Controller Refresh Cycle

7.1 386™SL CPU Timing Diagrams (Continued)



Entering External Master Mode

Exiting External Master Mode

Byte Swap Delay—External Master Read from an 8-Bit Resource

Byte Swap Delay—External Master Write to an 8-Bit Resource

Figure 7.1.27. ISA Bus External Bus Master

7.1 386™SL CPU Timing Diagrams (Continued)

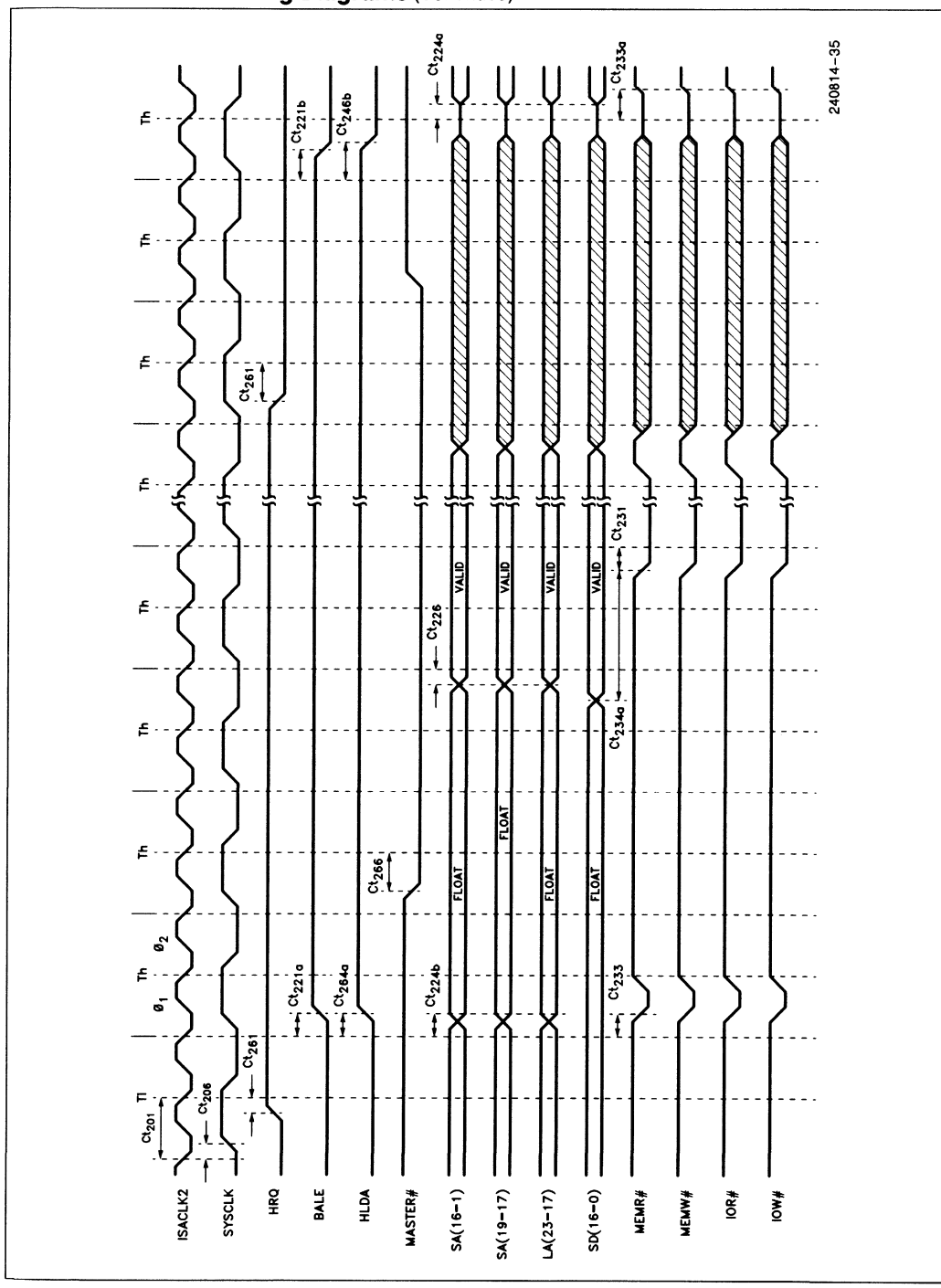
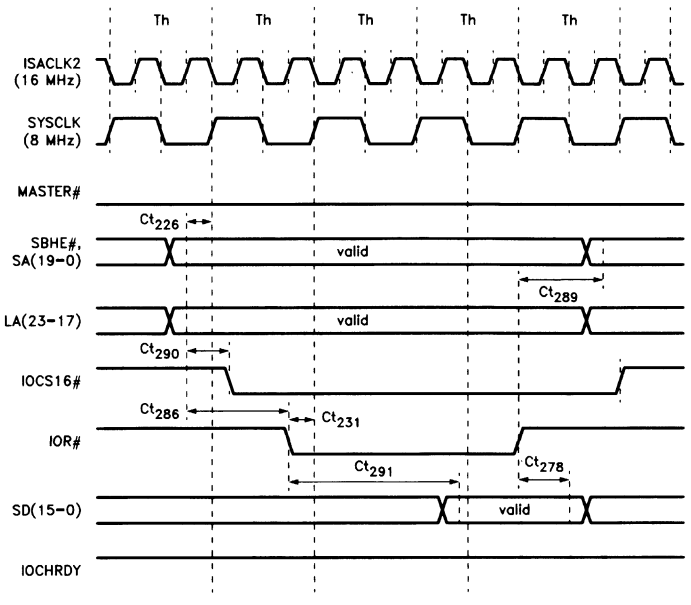
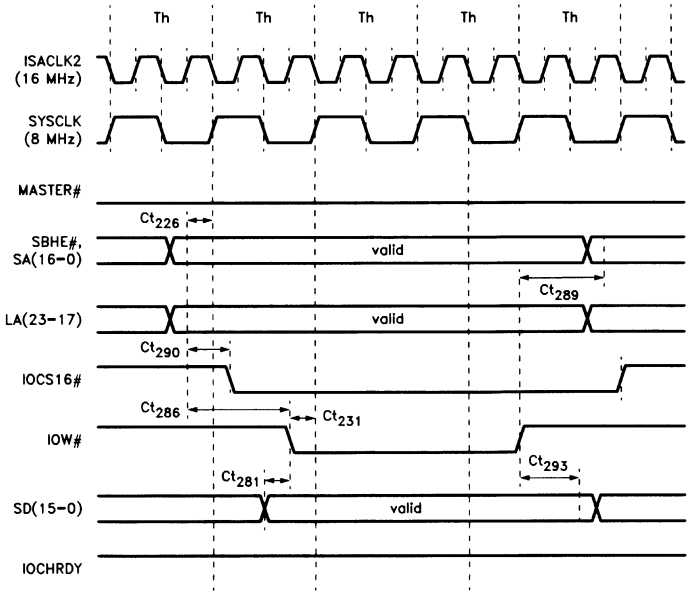


Figure 7.1.28. ISA Bus External Bus Master to Off-Board I/O Ports (No Byte-Swapping)

7.1 386™SL CPU Timing Diagrams (Continued)



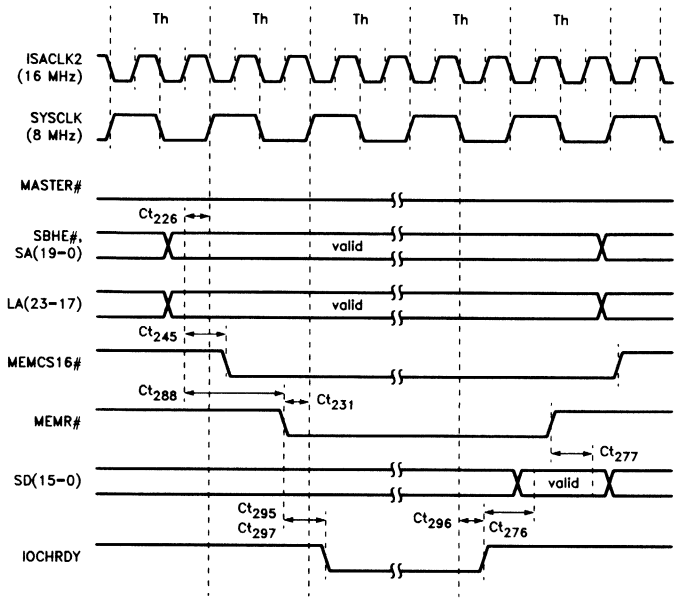
External Master Read from On-Board I/O Ports



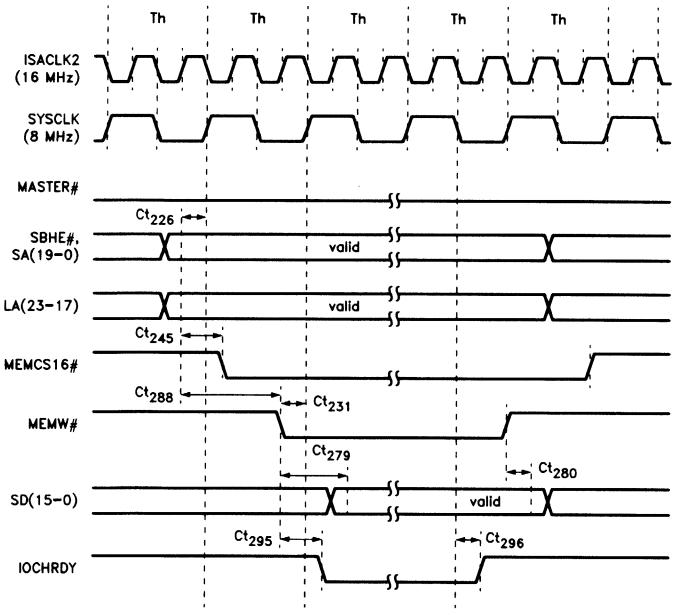
External Master Write to On-Board I/O Ports

Figure 7.1.29a. ISA Bus External Bus Master to On-Board I/O Ports (Read/Write)

7.1 386™SL CPU Timing Diagrams (Continued)



External Master Read from On-Board Memory



External Master Write to On-Board Memory

Figure 7.1.29b. ISA Bus External Bus Master Accesses to On-Board Memory

7.1 386™SL CPU Timing Diagrams (Continued)

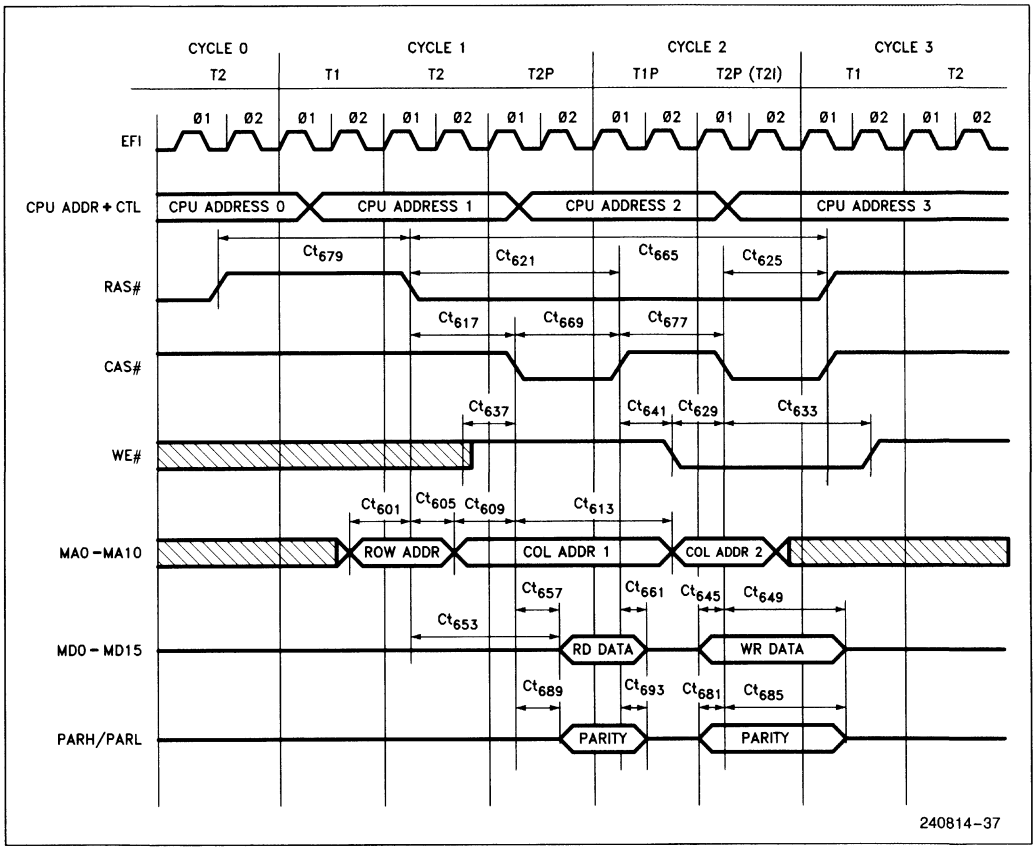


Figure 7.1.30. 386™SL CPU Memory Controller Timings (DRAM F1 Mode Timing Parameters)

7.1 386™SL CPU Timing Diagrams (Continued)

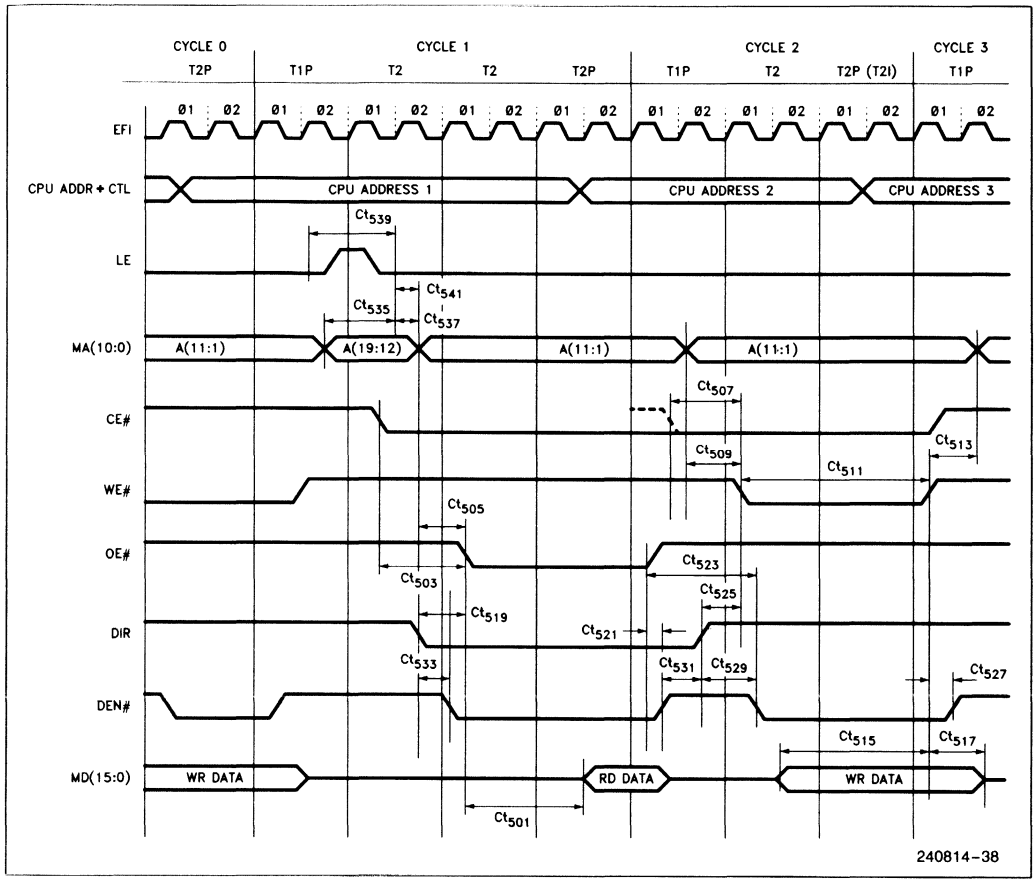


Figure 7.1.31. 386™SL CPU Memory Controller Timings (SRAM Mode Timing Parameters; 2 Wait States)

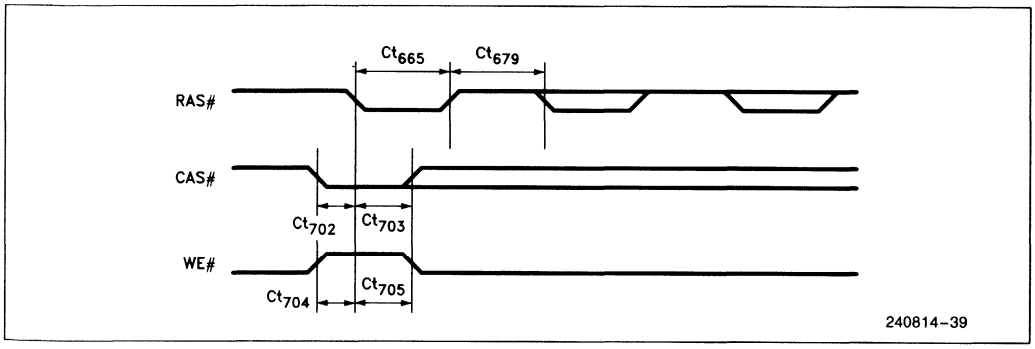


Figure 7.1.32. 386™SL CPU Memory Controller Timings (CAS# before RAS# Refresh Timings)

7.1 386™SL CPU Timing Diagrams (Continued)

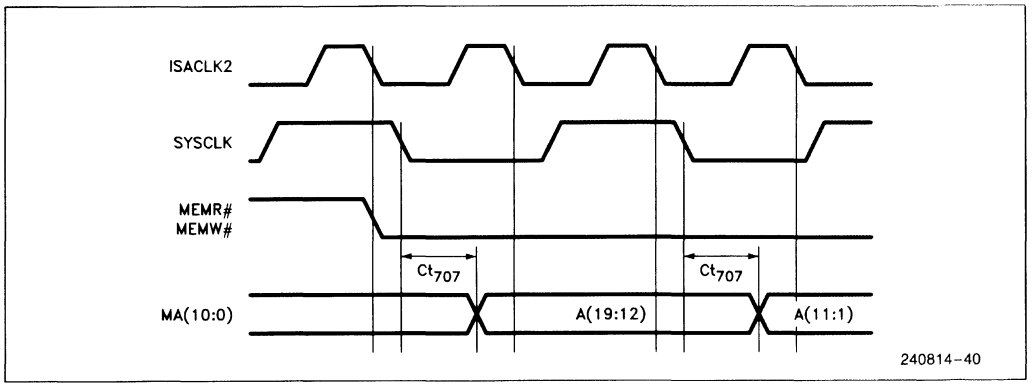


Figure 7.1.33. REFRESH, DMA/MASTER Timing Diagrams (Address Active Delay from SYSCLK)

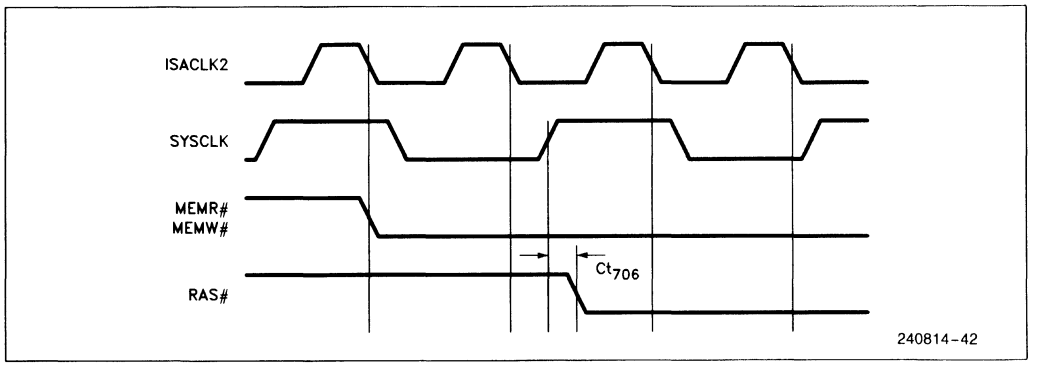


Figure 7.1.34. REFRESH, DMA/MASTER Timing Diagrams (RAS# Active Delay from SYSCLK)

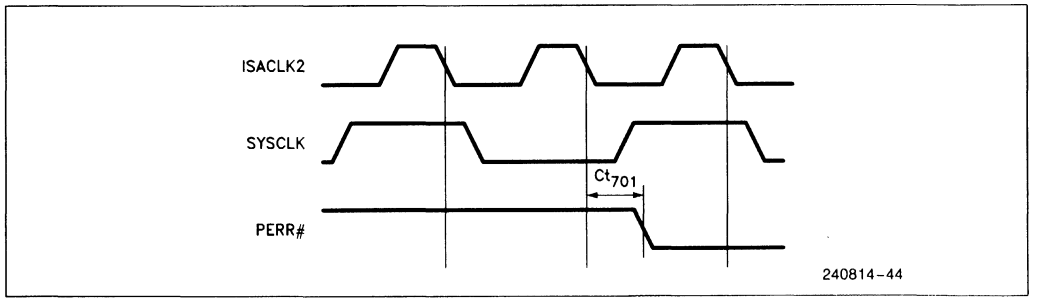


Figure 7.1.35. PERROR Timing Diagram (PERR# Active Delay from SYSCLK)

7.2 82360SL Timing Diagrams

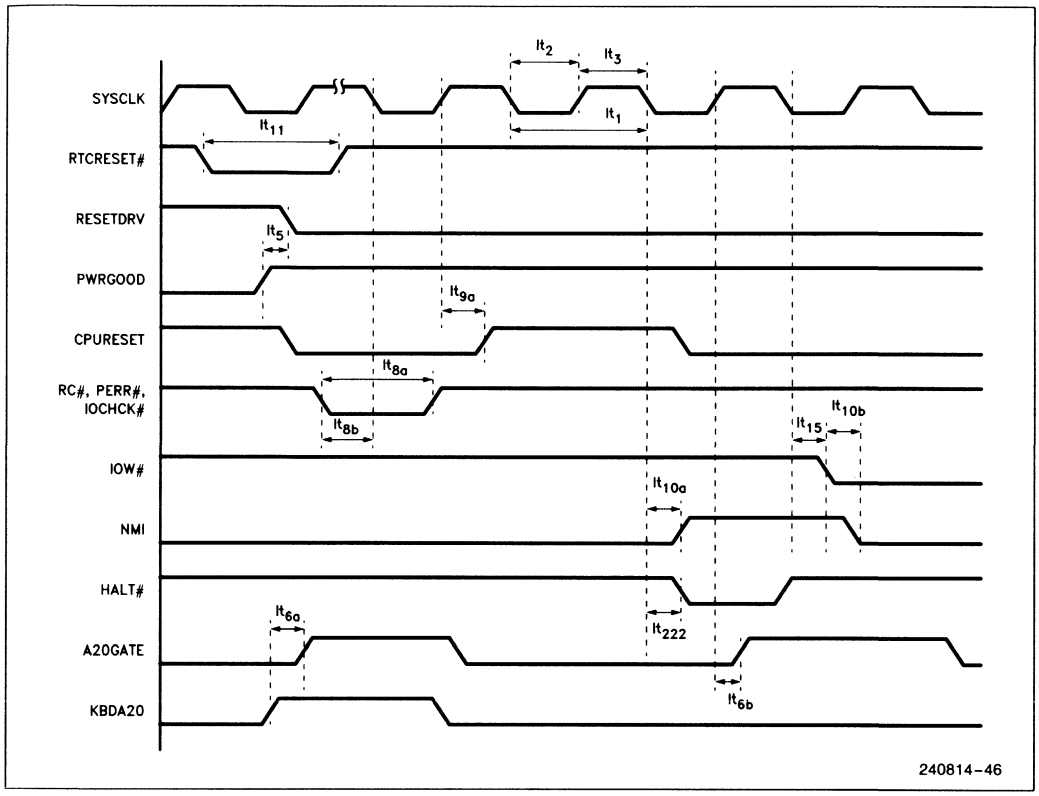


Figure 7.2.1. CPURESET, NMI, A20GATE and RC# Timings

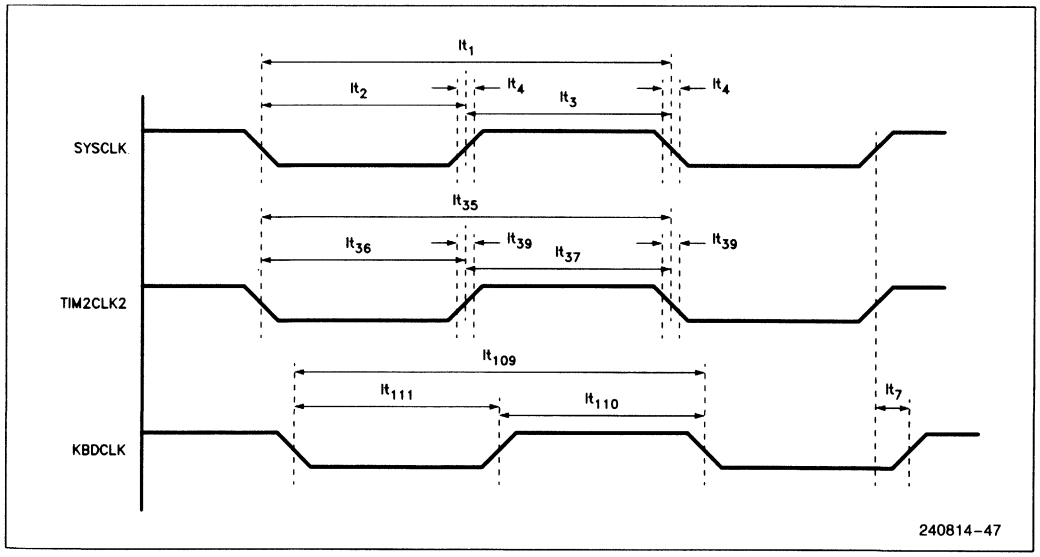


Figure 7.2.2. Clock Timings

7.2 82360SL Timing Diagrams (Continued)

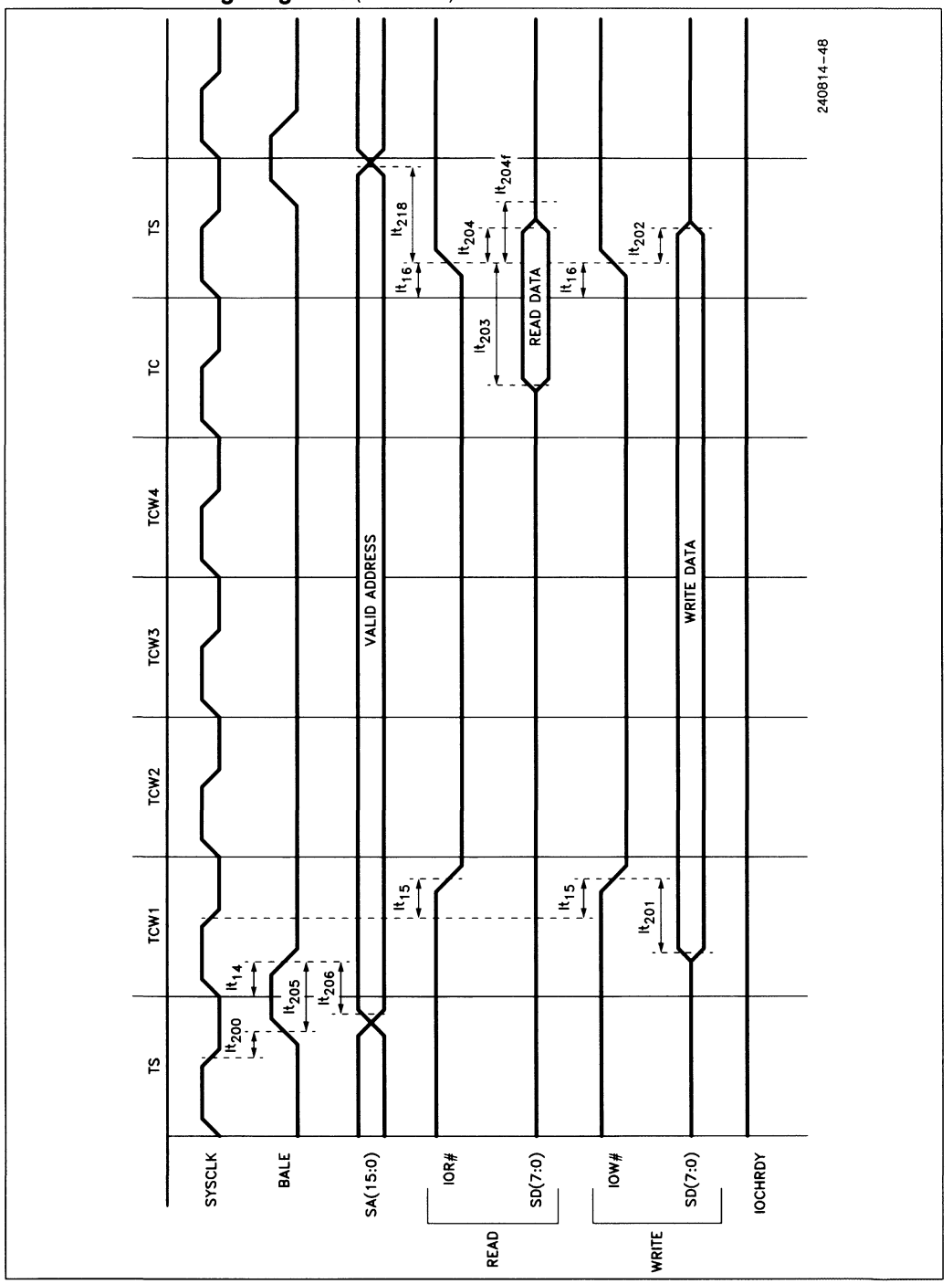


Figure 7.2.3. ISA Bus 8-Bit I/O Read/Write Default Bus Cycle (6 SYSCLKs)

7.2 82360SL Timing Diagrams (Continued)

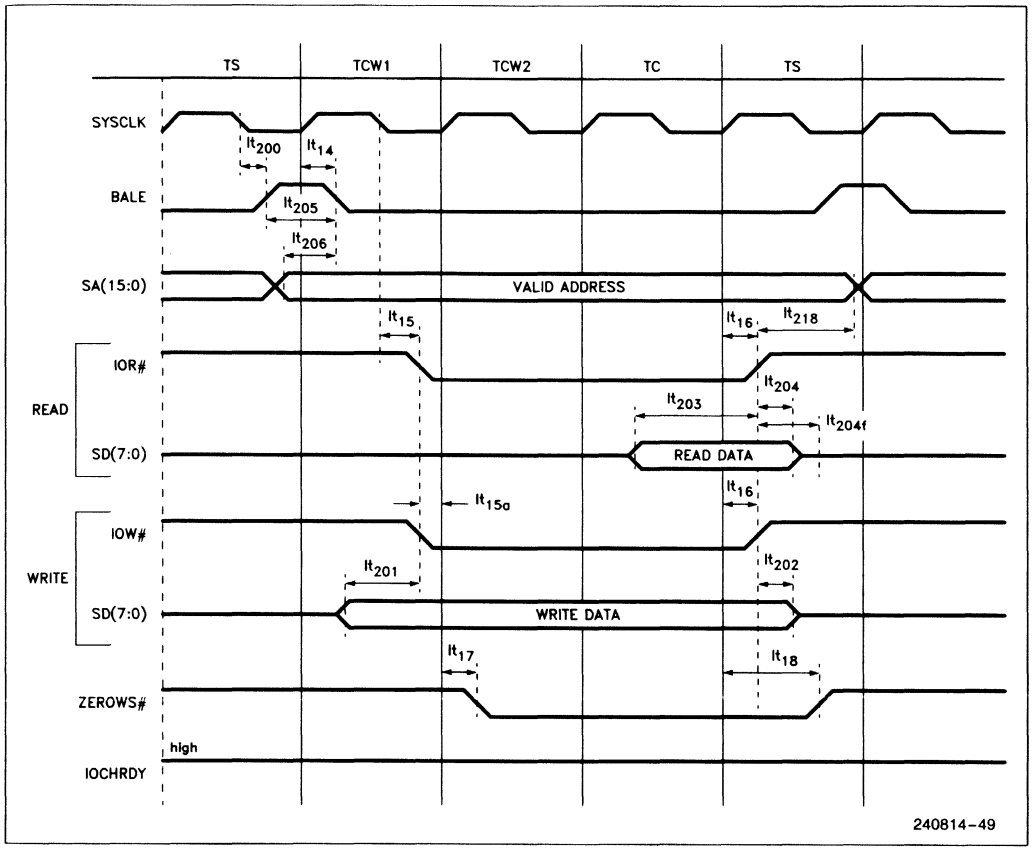


Figure 7.2.4. ISA Bus 8-Bit I/O Read/Write Compressed Bus Cycle

7.2 82360SL Timing Diagrams (Continued)

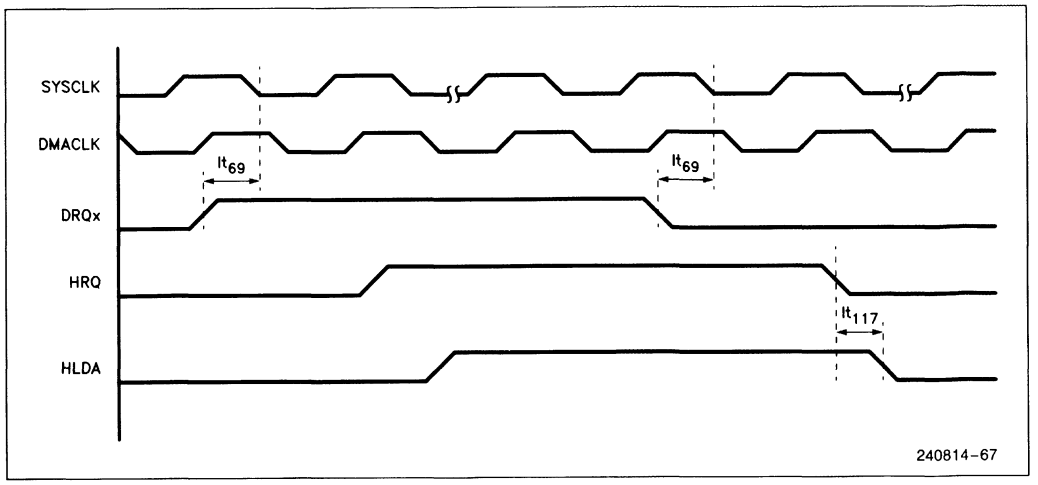


Figure 7.2.5. DMA Controller Timings

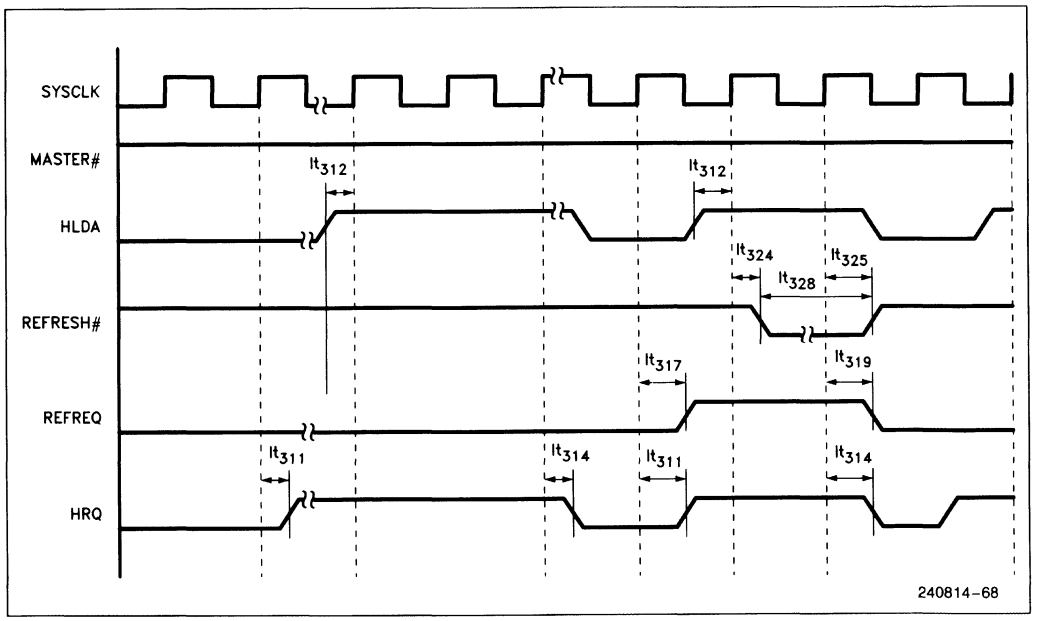


Figure 7.2.6. Refresh Arbitration Timings

7.2 82360SL Timing Diagrams (Continued)

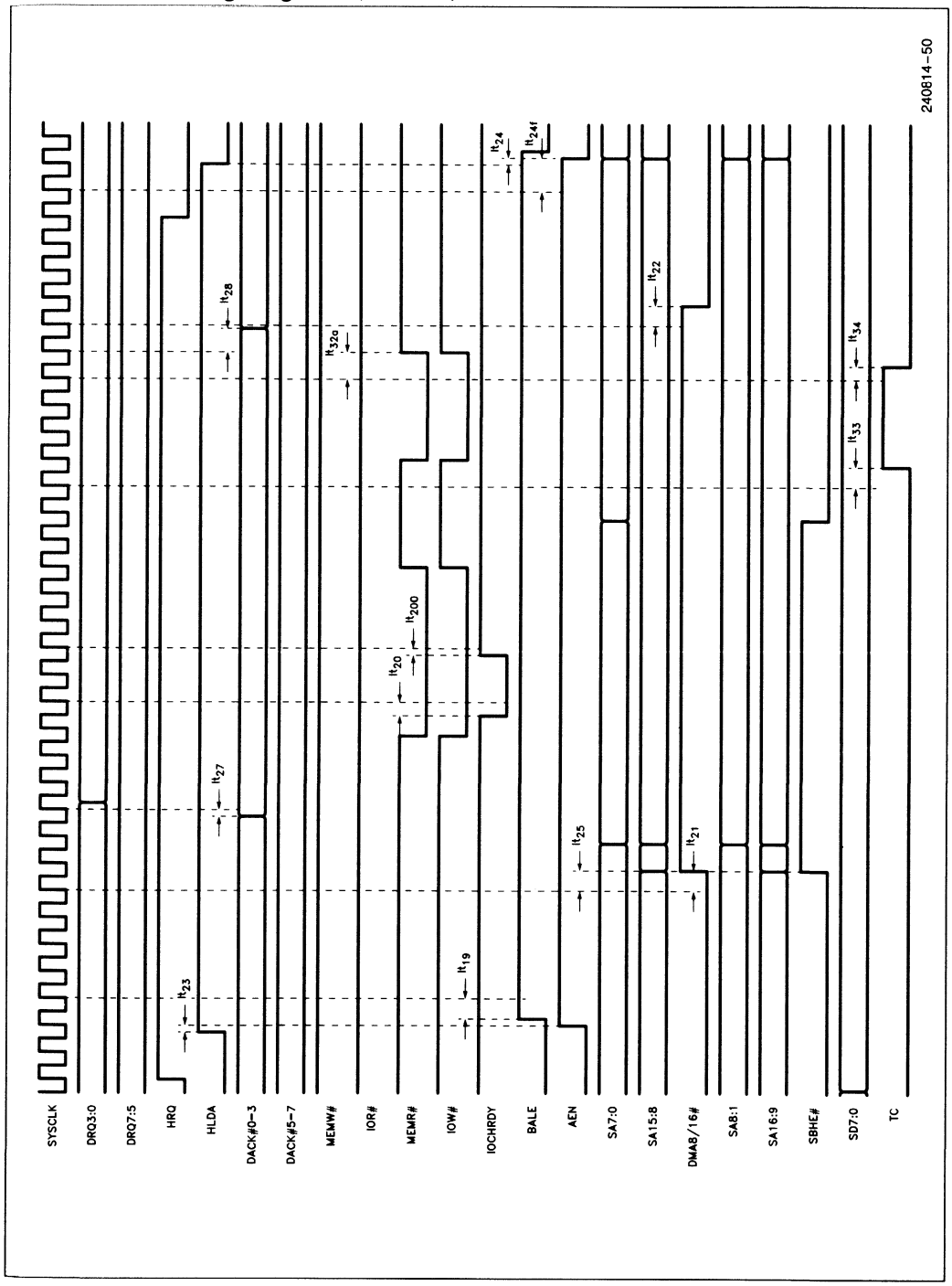


Figure 7.2.7. DMA Memory Write Timings

7.2 82360SL Timing Diagrams (Continued)

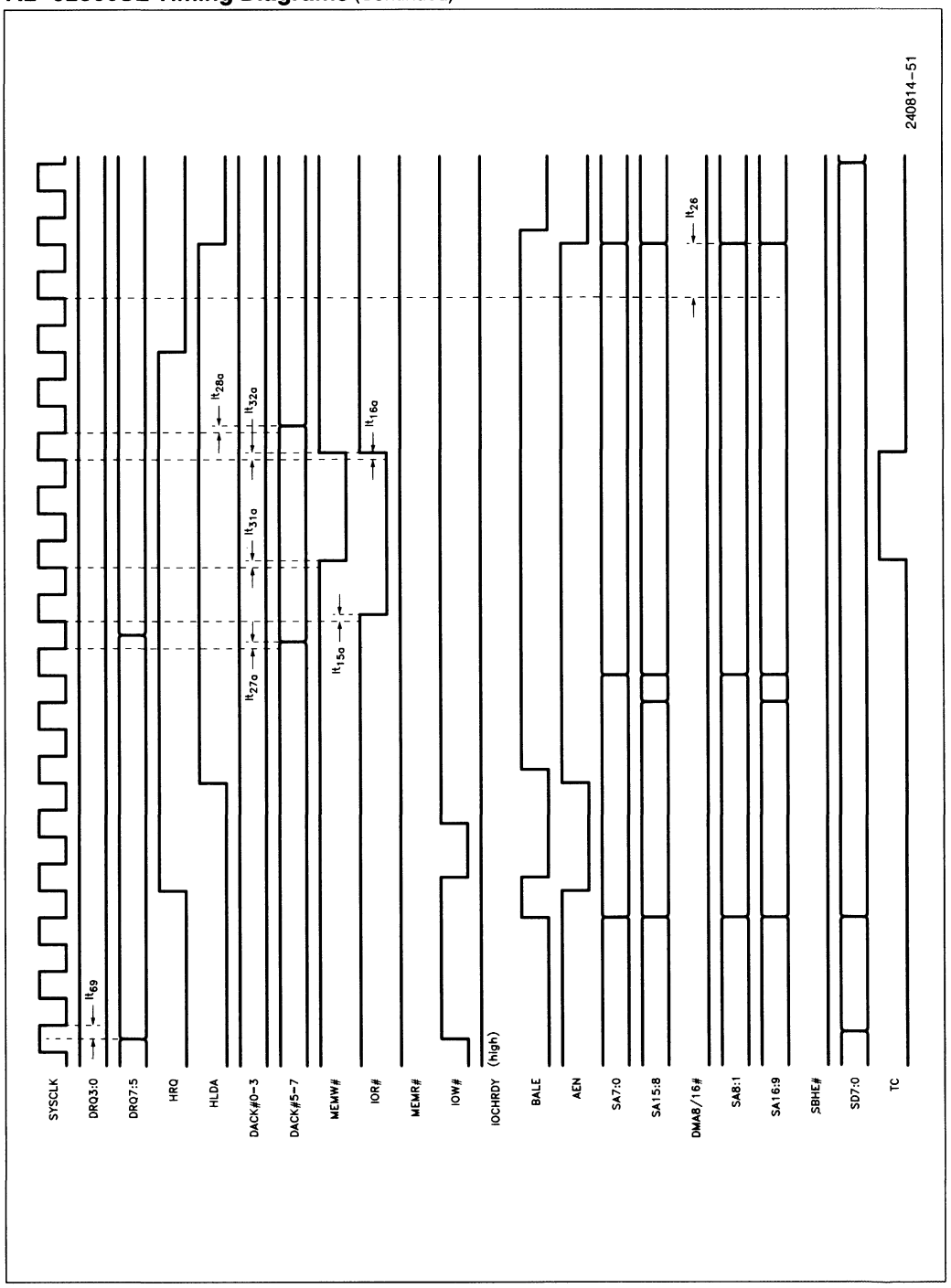


Figure 7.2.8. DMA Memory Read Timings

7.2 82360SL Timing Diagrams (Continued)

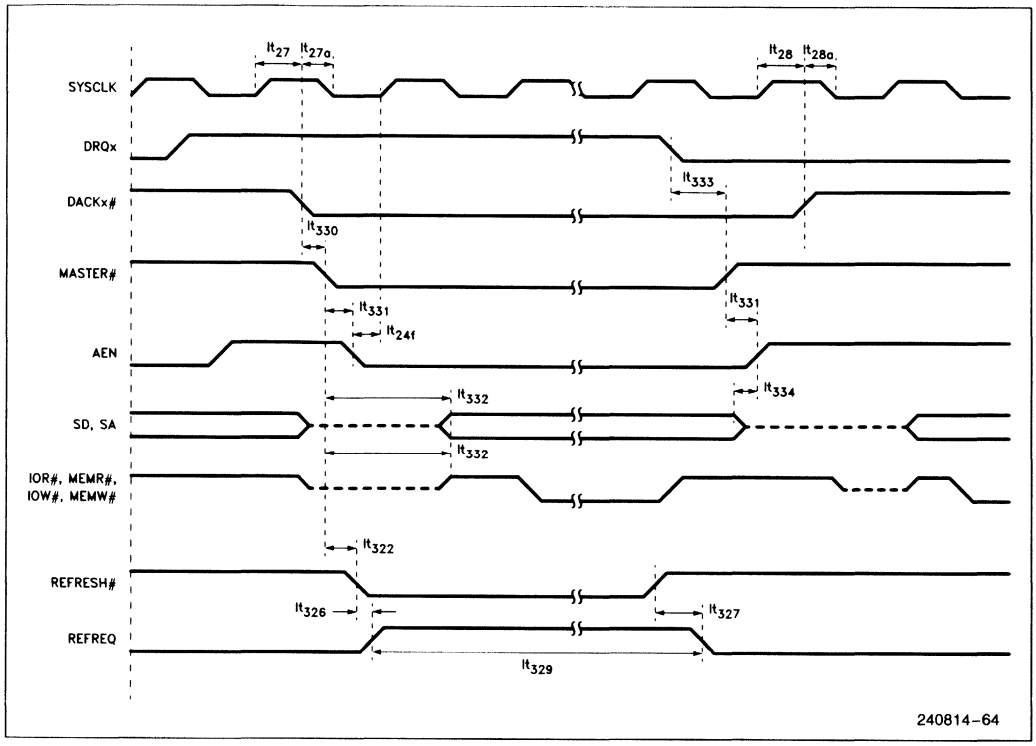


Figure 7.2.9. Bus Master Refresh Cycle Timings

7.2 82360SL Timing Diagrams (Continued)

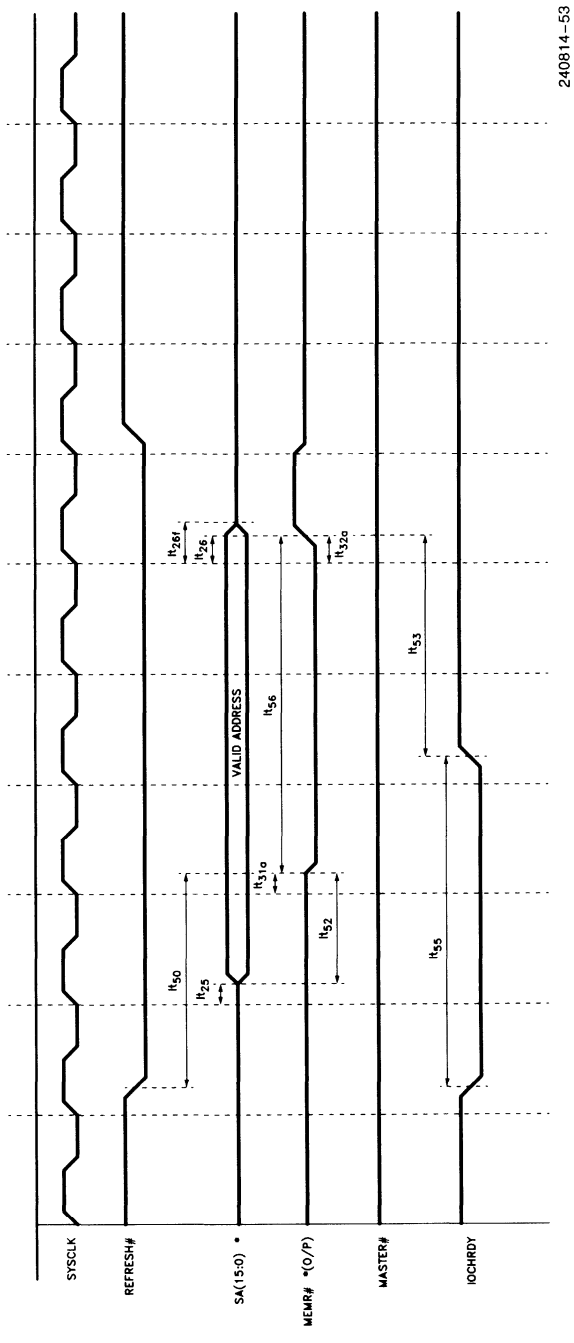


Figure 7.2.10. ISA Bus Master Refresh Cycle with IOCHRDY Timings

7.2 82360SL Timing Diagrams (Continued)

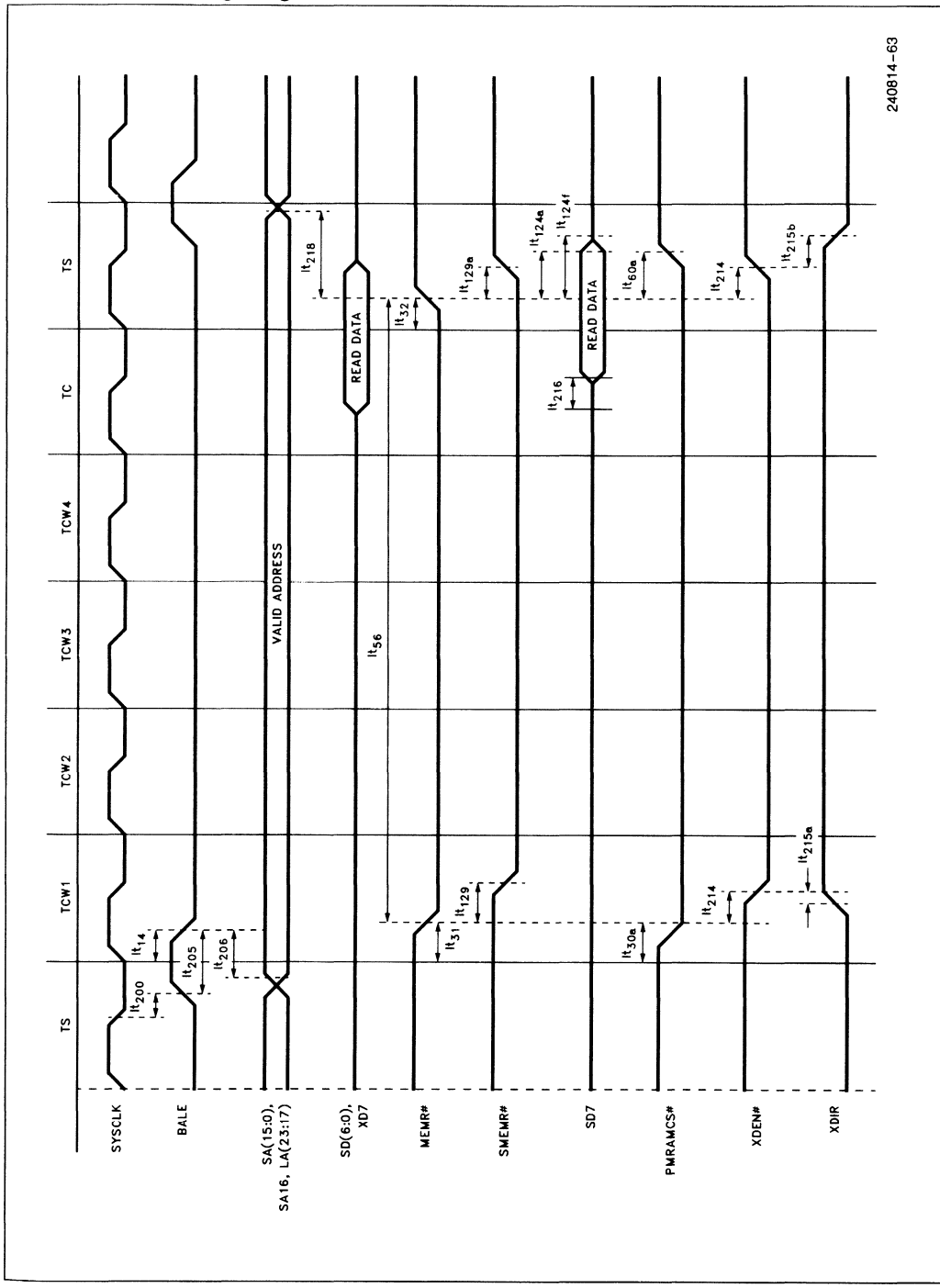


Figure 7.2.11. X-Bus Control Signals—Memory Read Timings

7.2 82360SL Timing Diagrams (Continued)

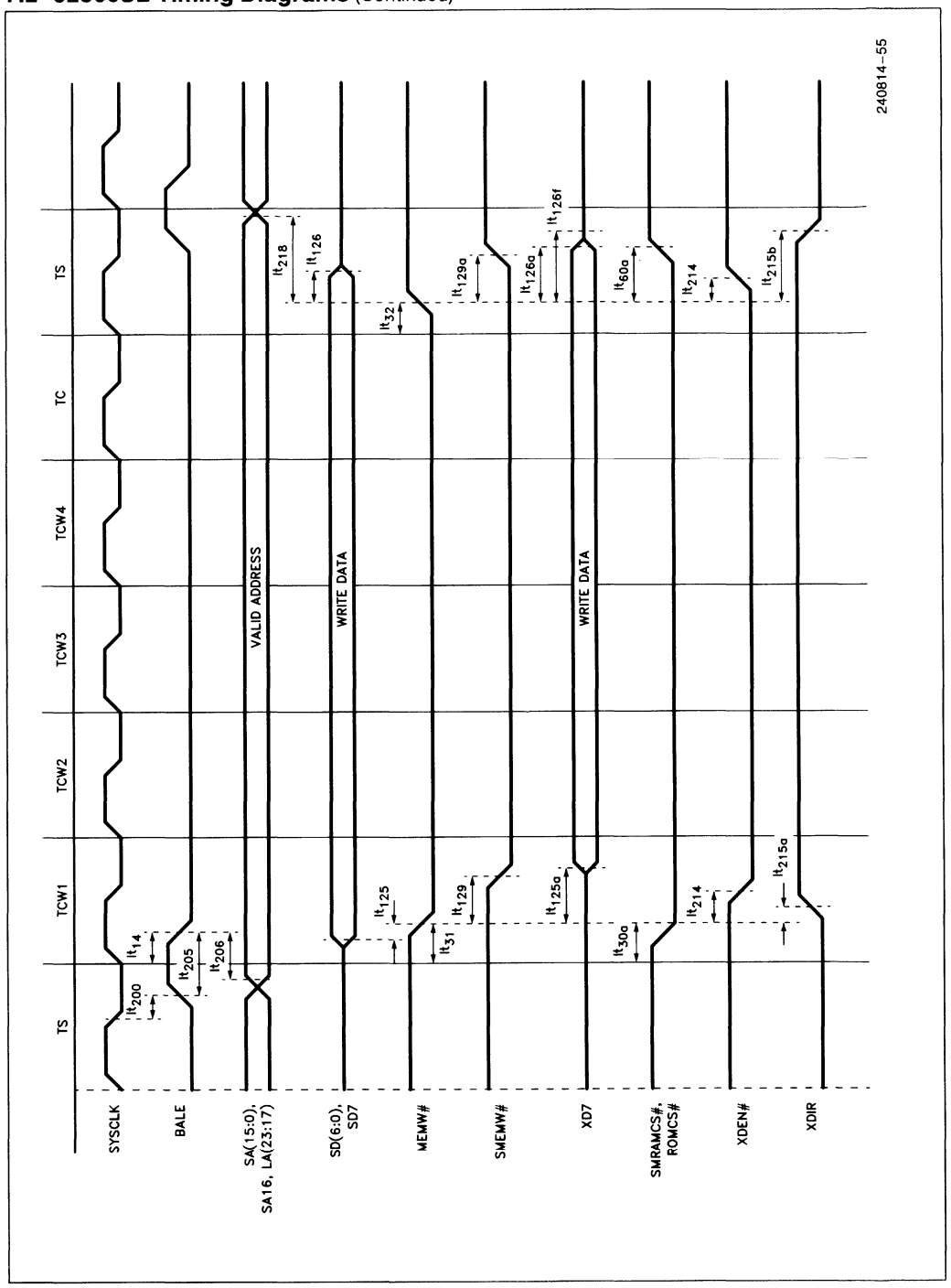


Figure 7.2.12. X-Bus Control Signals—Memory Write Timings

7.2 82360SL Timing Diagrams (Continued)

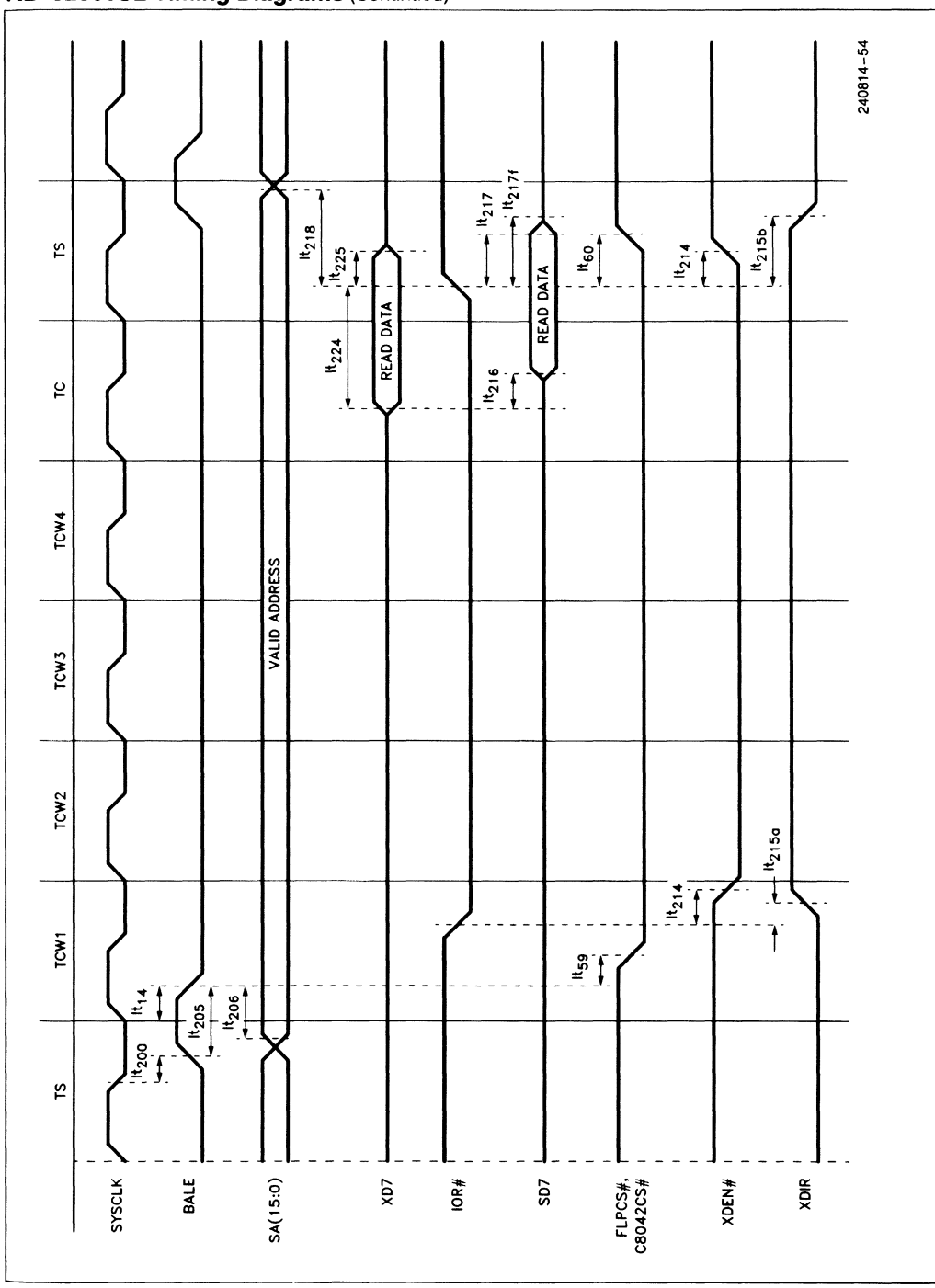


Figure 7.2.13. X-Bus Control Signals—I/O Read Timings

7.2 82360SL Timing Diagrams (Continued)

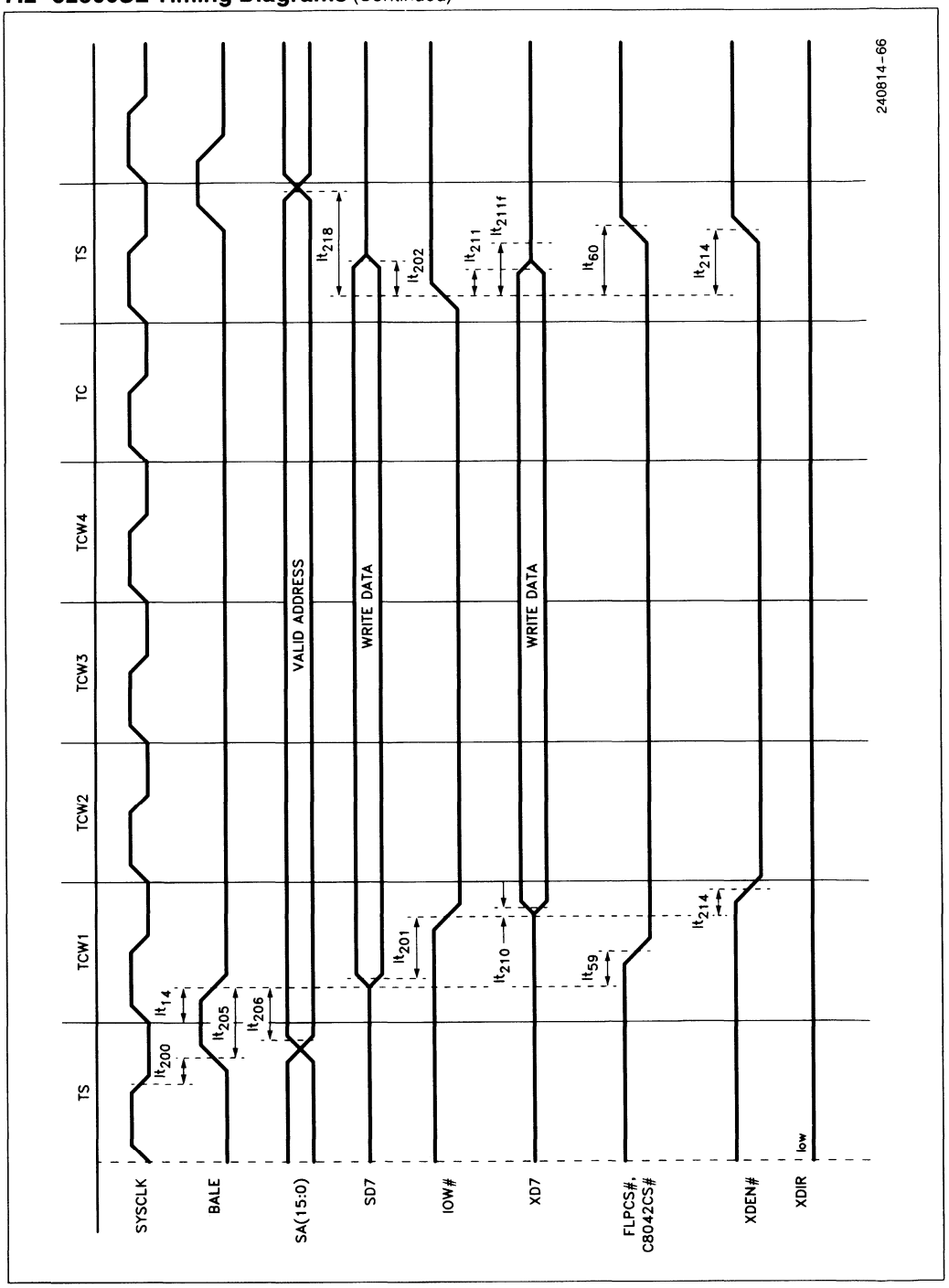


Figure 7.2.14. X-Bus Control Signals—I/O Write Timings

7.2 82360SL Timing Diagrams (Continued)

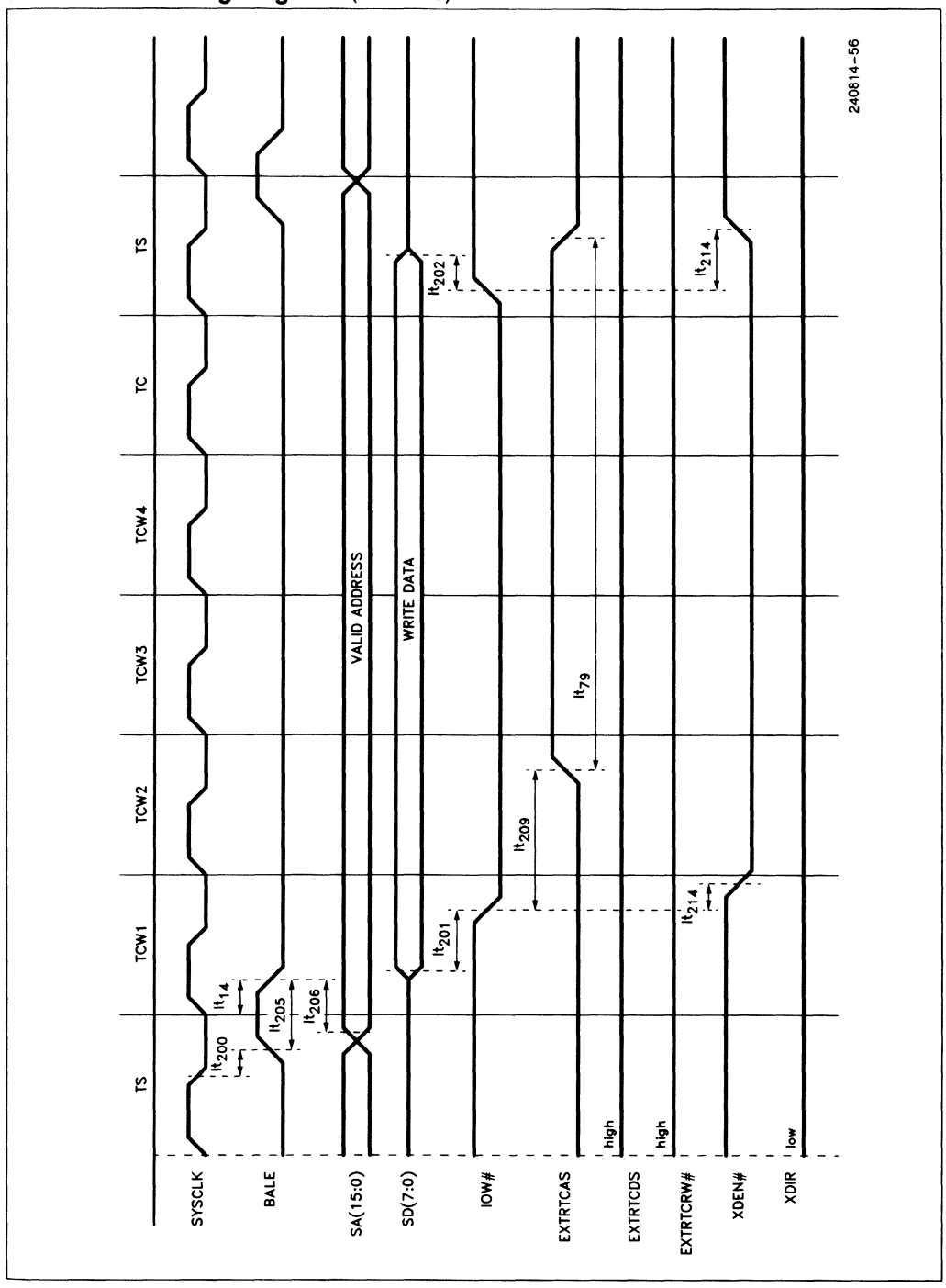


Figure 7.2.15. I/O Port 70 Hex Write—External RTC Timings

7.2 82360SL Timing Diagrams (Continued)

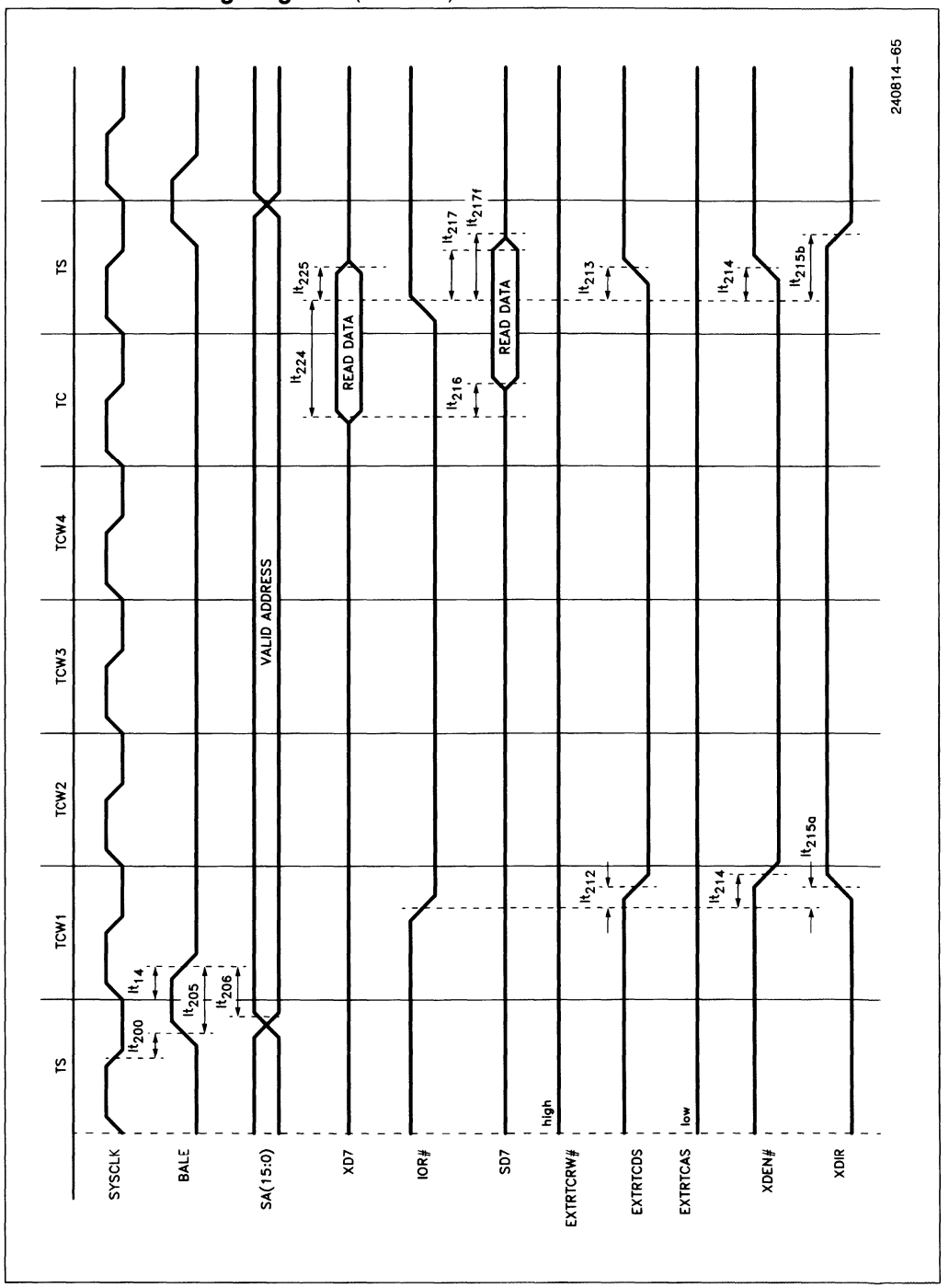


Figure 7.2.16. I/O Port 71 Hex Read—External RTC Timings

7.2 82360SL Timing Diagrams (Continued)

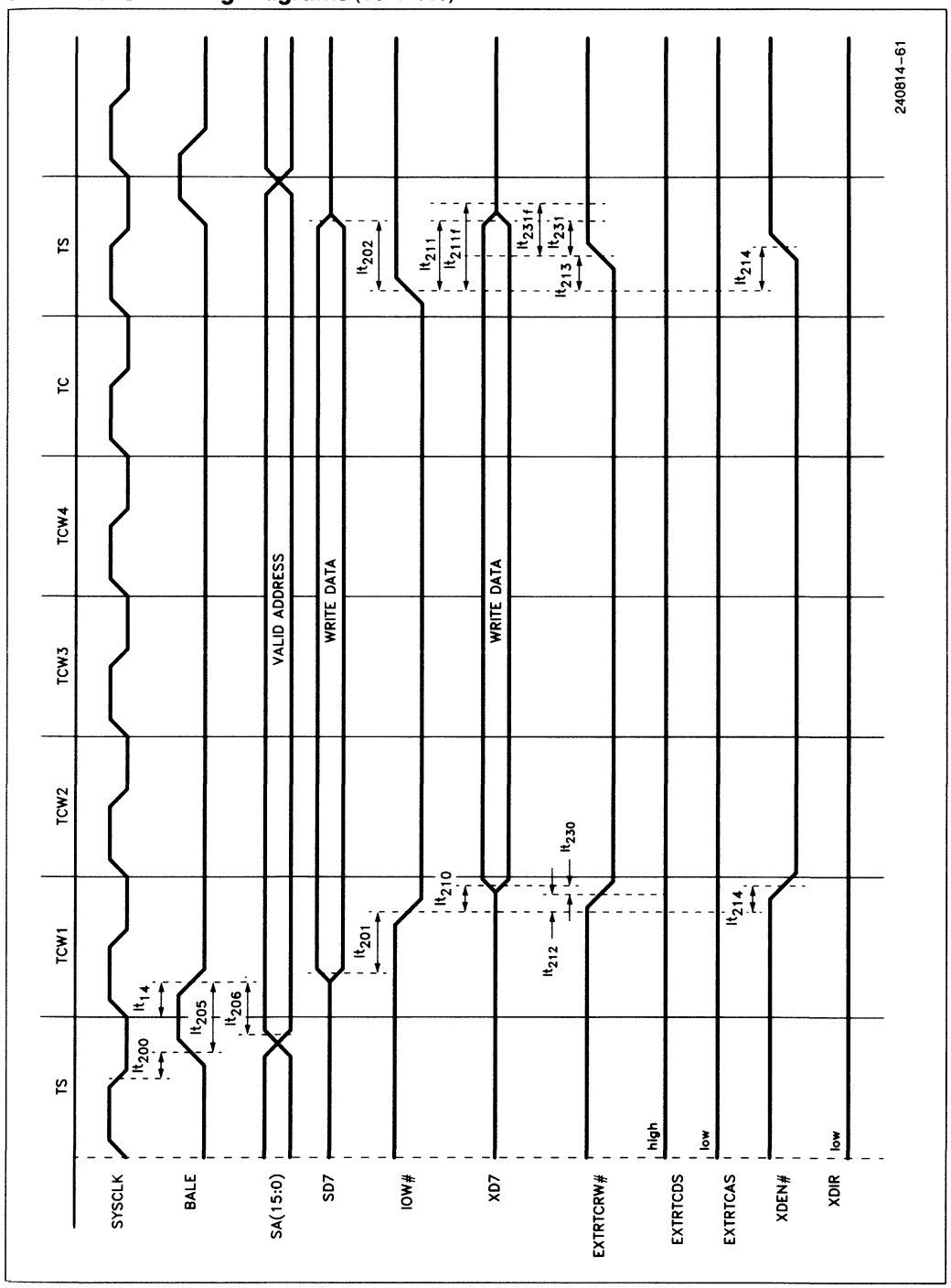


Figure 7.2.17. I/O Port 71 Hex Write—External RTC Timings

7.2 82360SL Timing Diagrams (Continued)

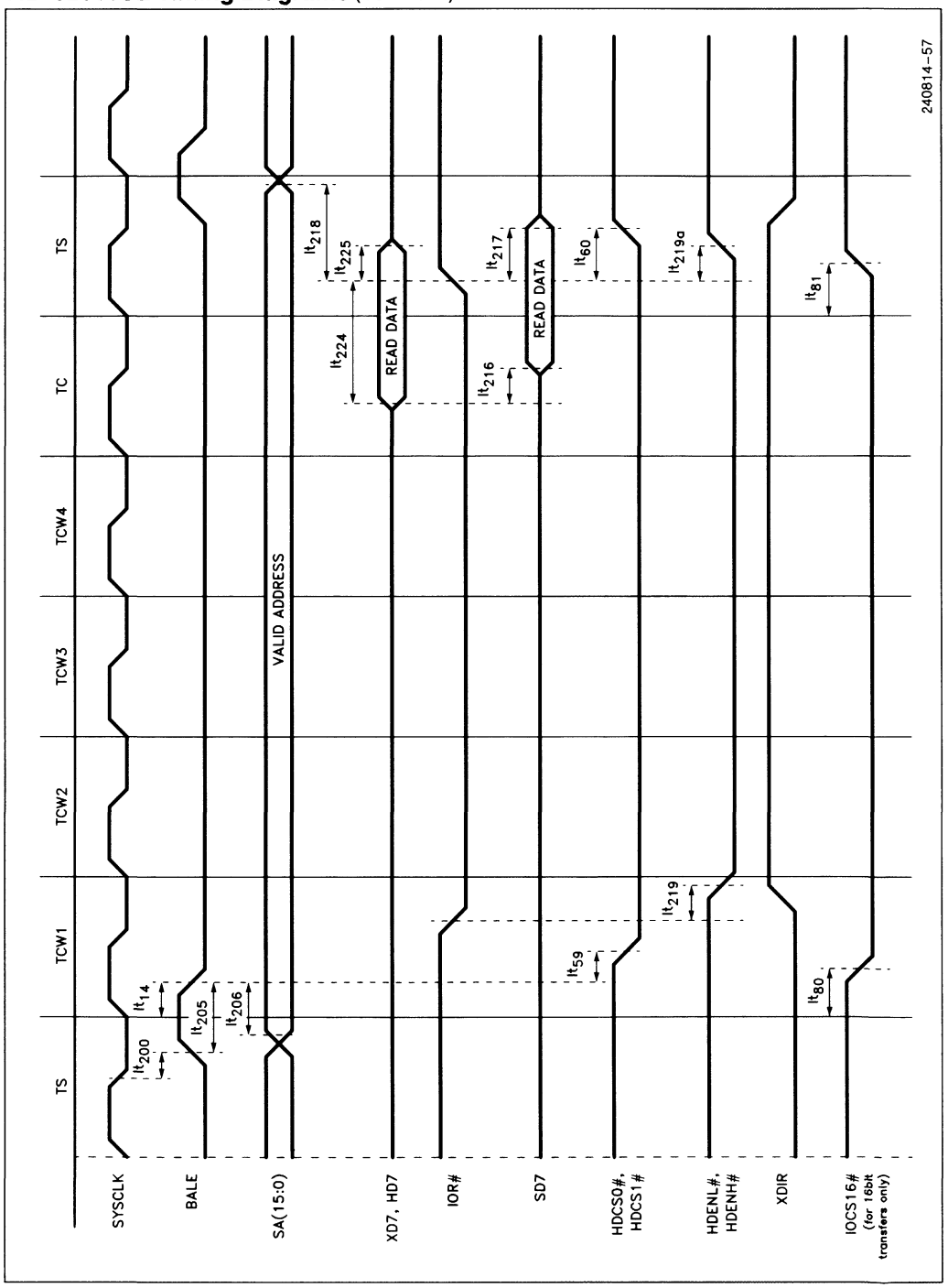


Figure 7.2.18. I.D.E. Hard Disk Control Signals—I/O Read Timings

7.2 82360SL Timing Diagrams (Continued)

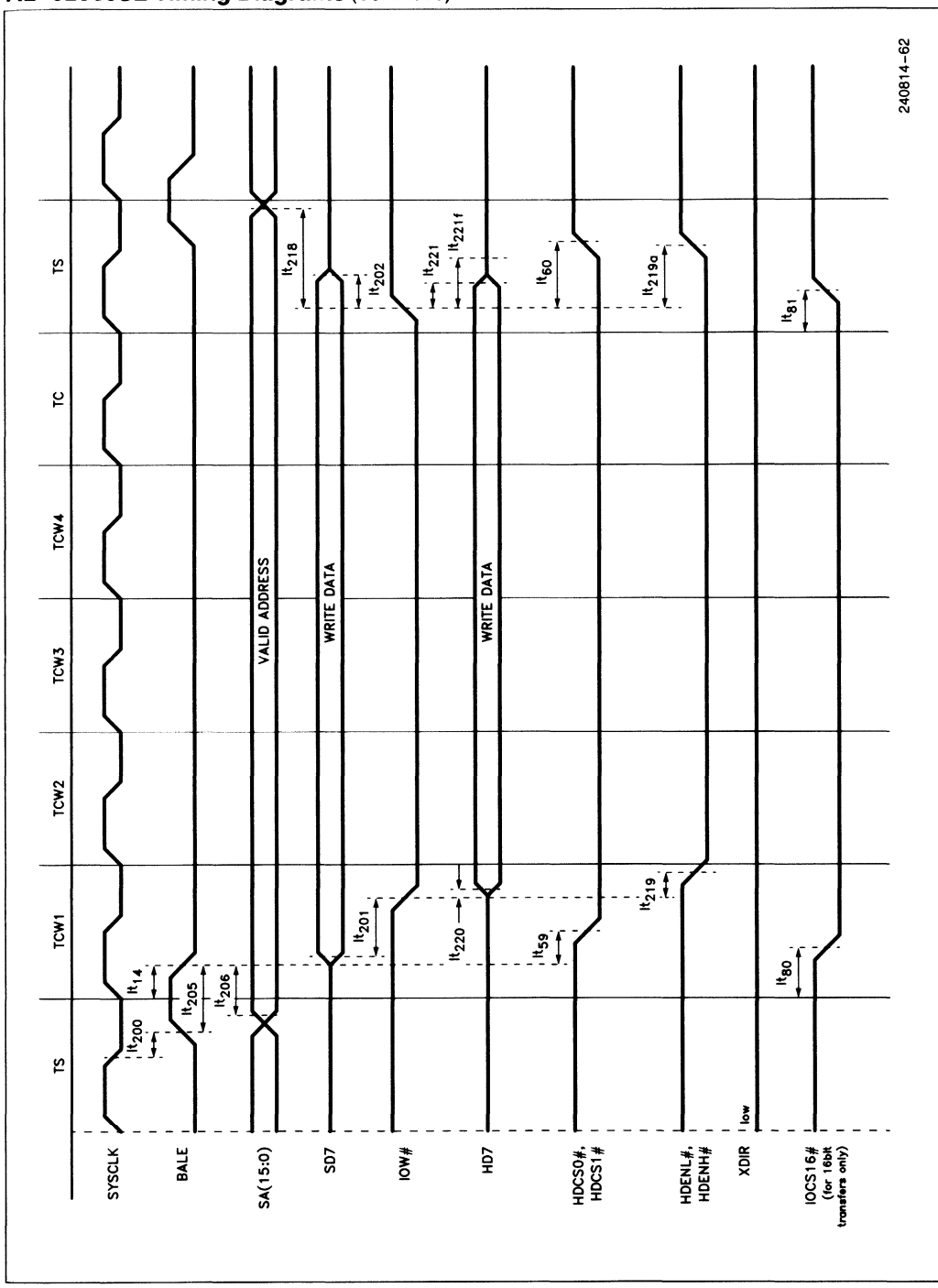


Figure 7.2.19. I.D.E. Hard Disk Control Signals—I/O Write Timings

7.2 82360SL Timing Diagrams (Continued)

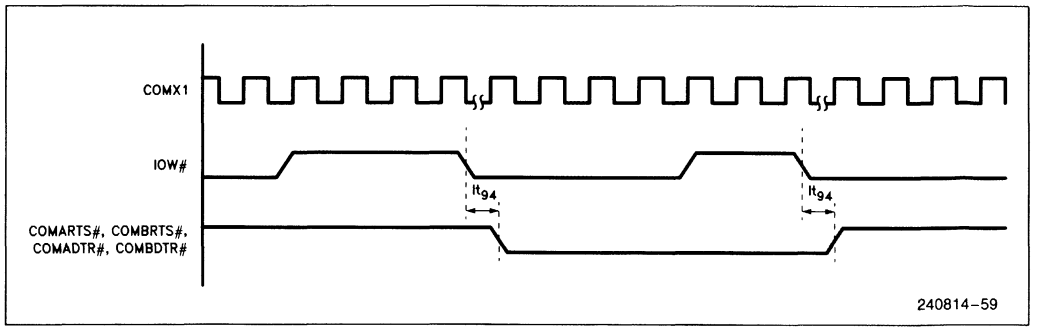


Figure 7.2.20. Serial Port Controller—Modem Control Signal Timings

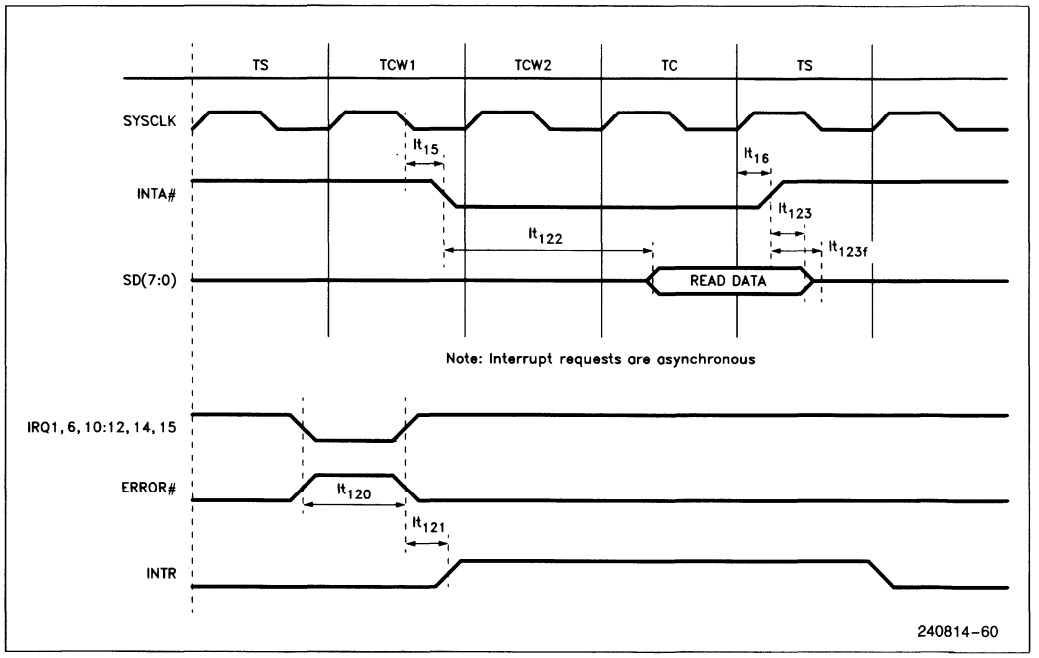


Figure 7.2.21. Interrupt Controller Timings

7.2 82360SL Timing Diagrams (Continued)

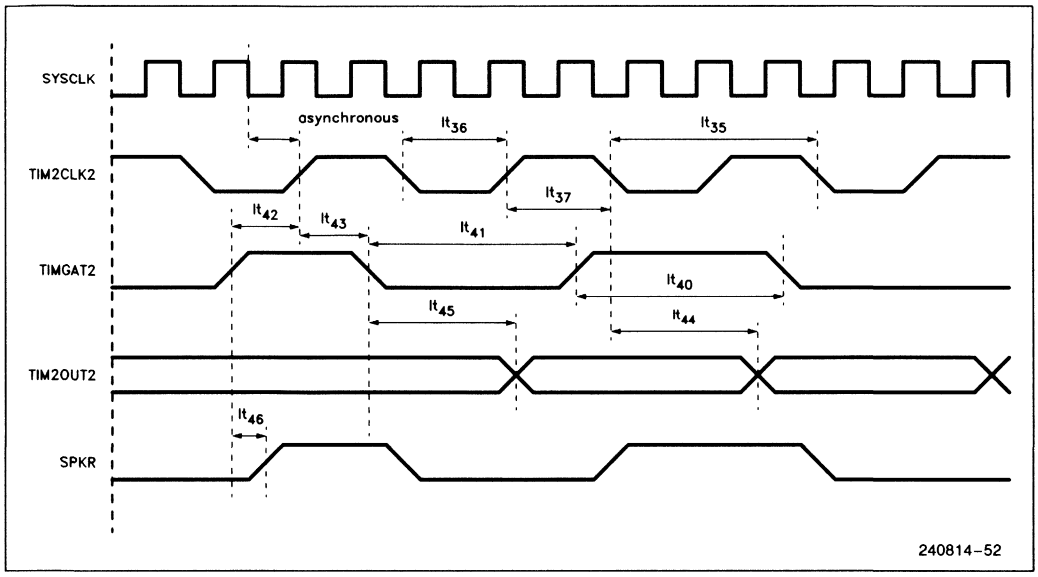


Figure 7.2.22. Programmable Interval Timer/Counter Timings

7.2 82360SL Timing Diagrams (Continued)

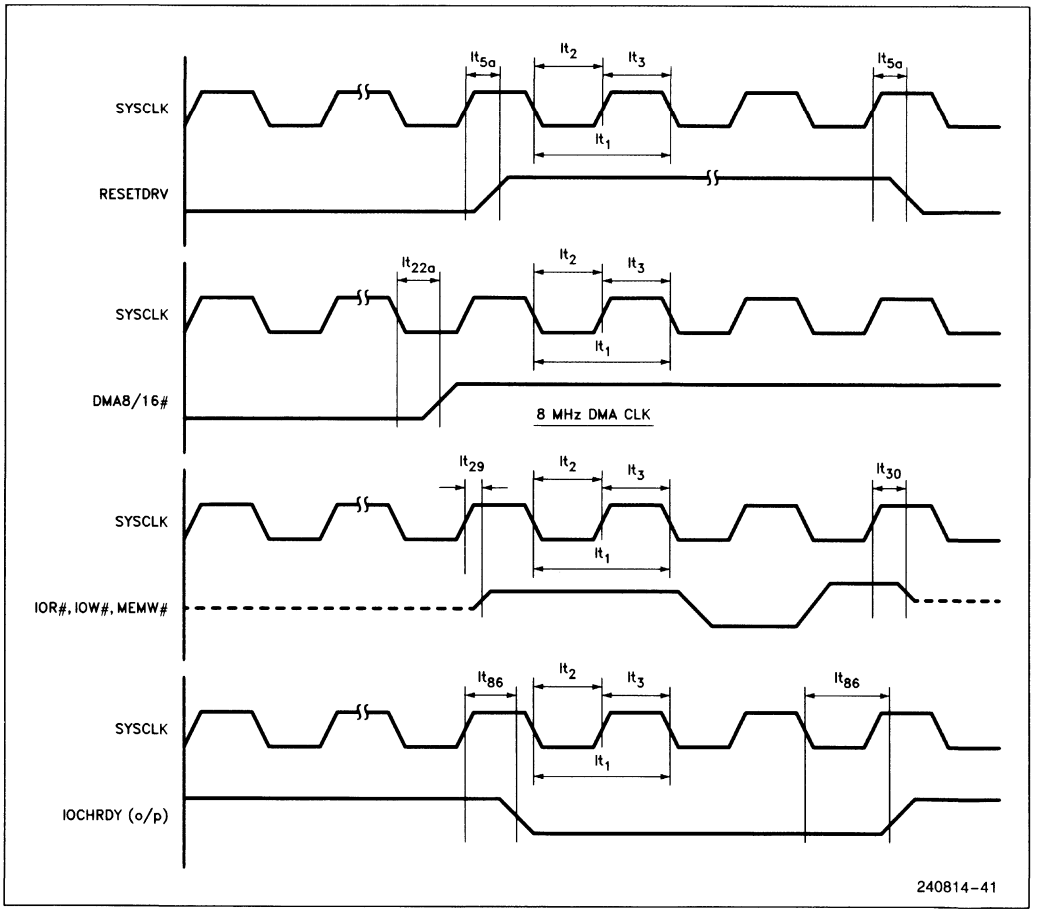


Figure 7.2.23. RESETDRV, DMA8/16#, Command Signals and IOCHRDY with Respect to SYSCLK

7.2 82360SL Timing Diagrams (Continued)

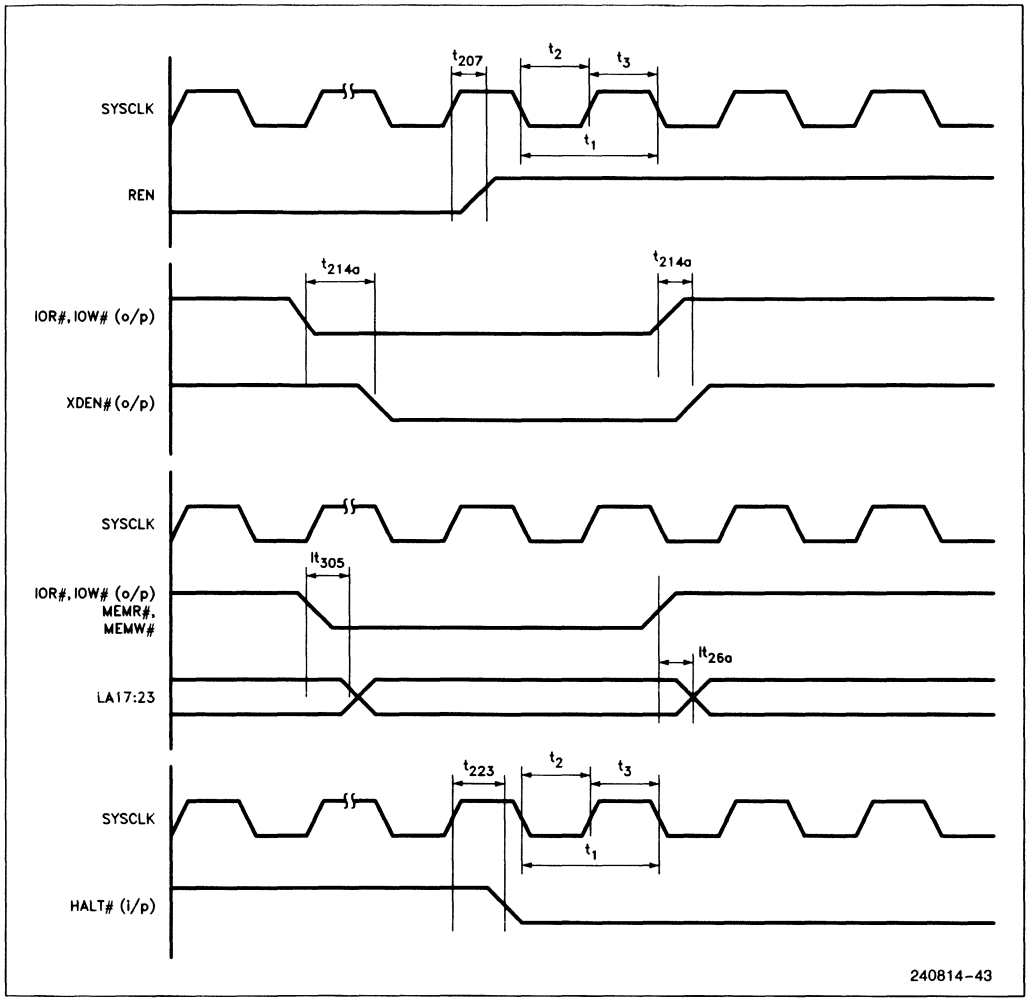


Figure 7.2.24. AEN and HALT with Respect to SYSCLK XDEN# and IOR#/IOW# with respect to LA17-23

7.2 82360SL Timing Diagrams (Continued)

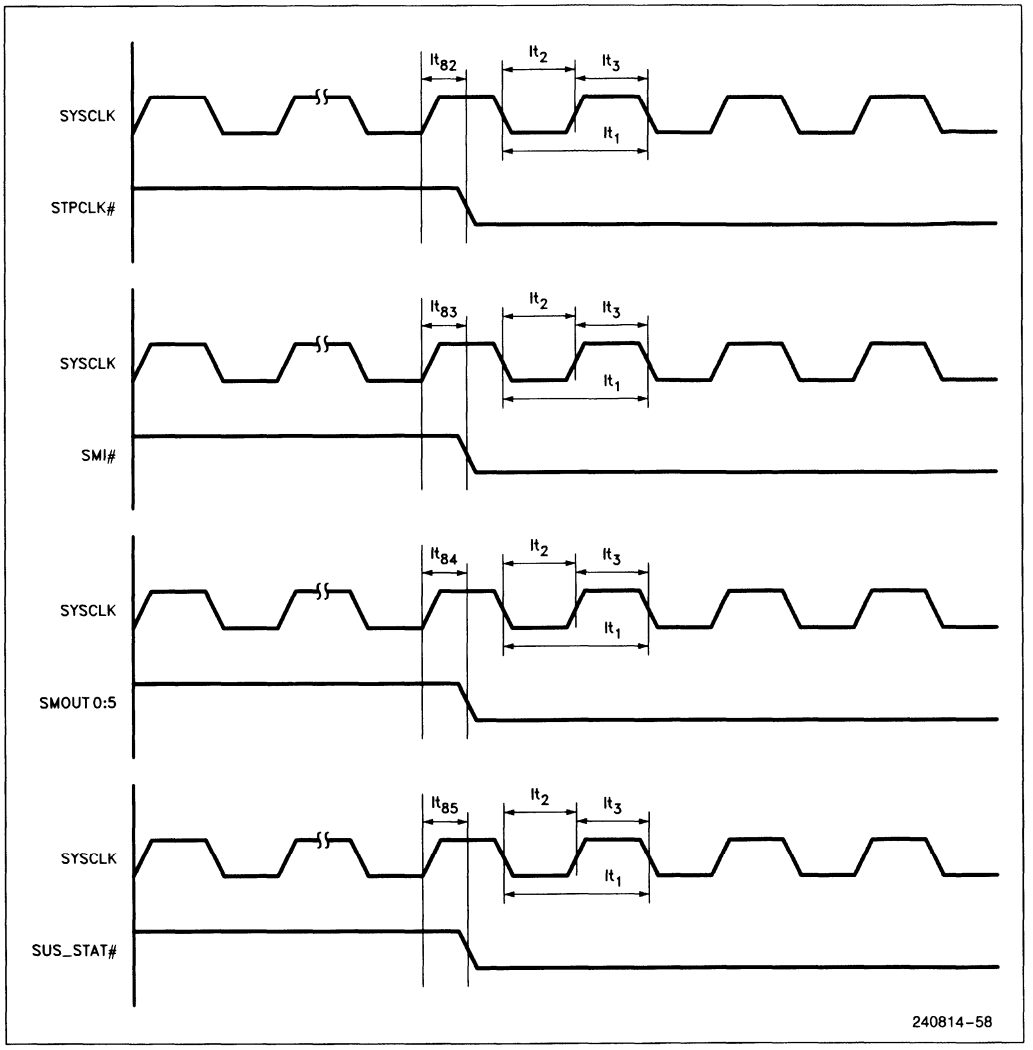


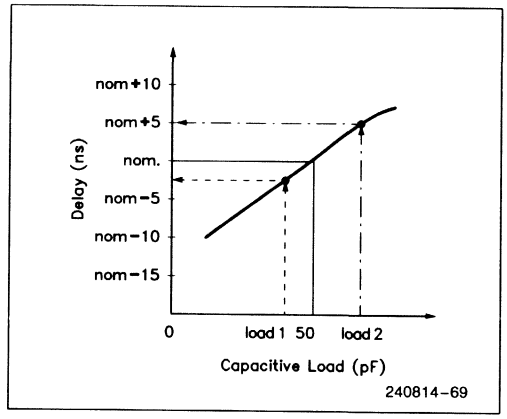
Figure 7.2.25. System Power Management Control Signal Timings

8.0 CAPACITIVE DERATING INFORMATION

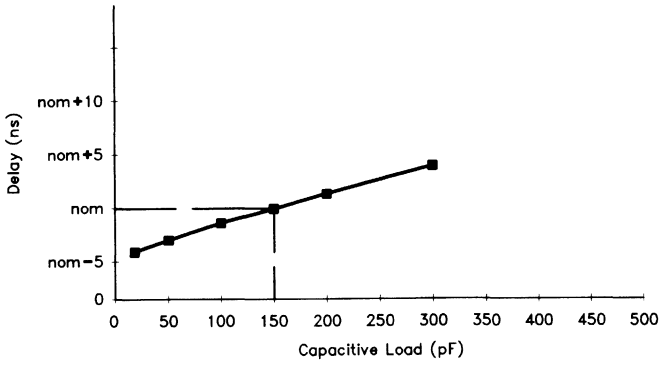
In the timing diagrams shown in the previous section, all maximum timings specified are at a maximum value of capacitive load tested on the signal pin. This maximum value is different for different pins and can be obtained for each pin from the pin assignment table in section 2. The delay introduced to signal transitions at the maximum specified load will be called the nominal delay. If, however, either a lighter or heavier capacitive load is connected to a pin, signal delay will change. To allow the system designer to account for such loading differences, capacitive derating curves have been provided in this section.

The derating curves for different pins depend on the internal buffers used. Nine derating curves are provided to account for the various classes of internal buffers used with different delay characteristics. To use these derating curves, follow the procedure outlined here.

1. From the Pin assignment chart, find the letter in the column "Derating Curve" corresponding to the signal under consideration.
2. In this section, find the derating curve of the correct type.
3. Calculate the capacitive loading on the signal under consideration.
4. Find this load point on the capacitive load axis of the derating curve.
5. Project a vertical line to the derating curve from the load point and draw a horizontal line from the point the vertical line intersects the curve.
6. Estimate the amount of time from the nominal point to the point where the horizontal line meets the delay axis. This is the derating value.
7. If the point where the horizontal meets the delay axis is above the nominal value, then this derating value should be **added** to signal timings shown in the timing diagrams. If the horizontal meets the delay axis below the nominal value, the derating value should be **subtracted** from the signal timings.
8. The derating curves shown can be used in identical manner for both rising and falling edges of the signal.

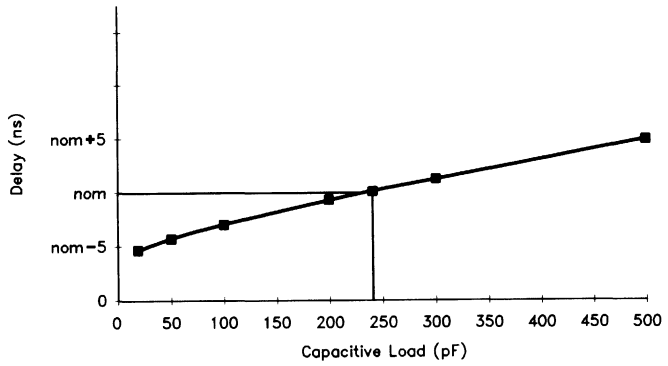


Using The Capacitive Derating Curves



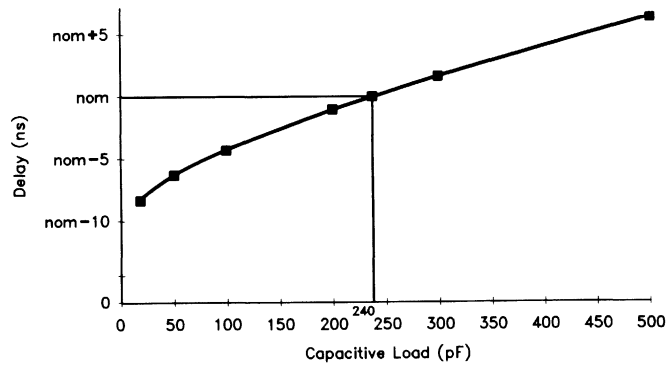
240814-70

Type A



240814-71

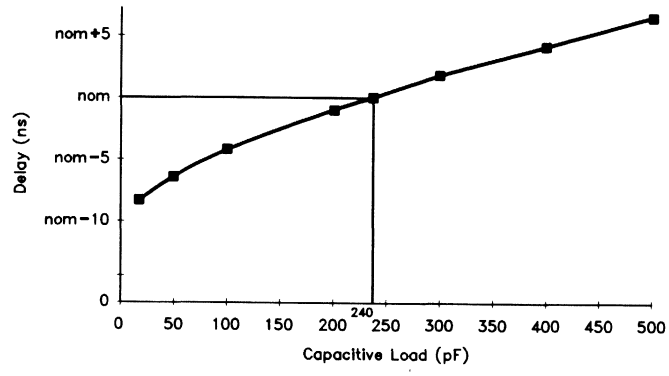
Type B



240814-72

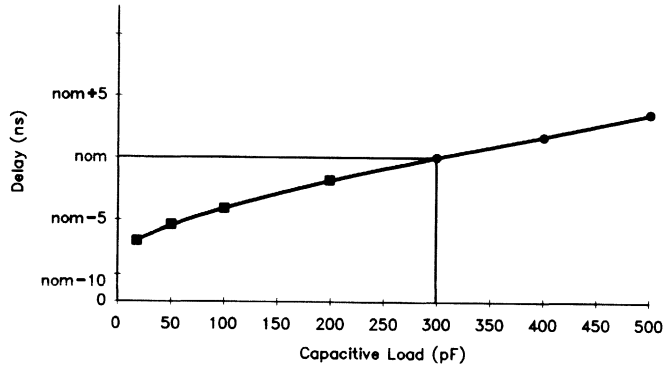
Type C

Capacitive Derating Curves



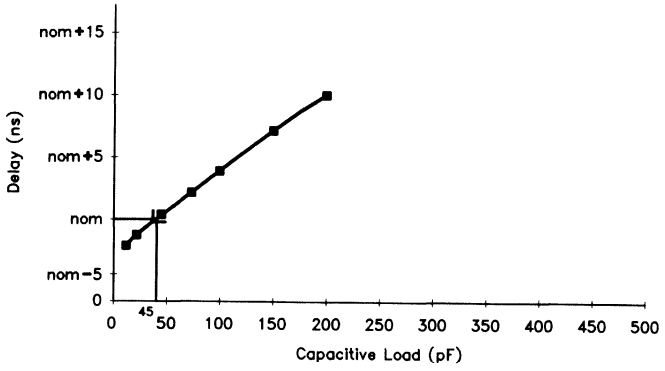
240814-73

Type D



240814-74

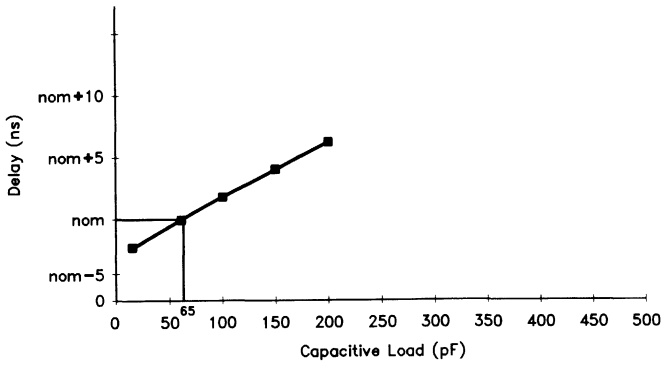
Type E



240814-75

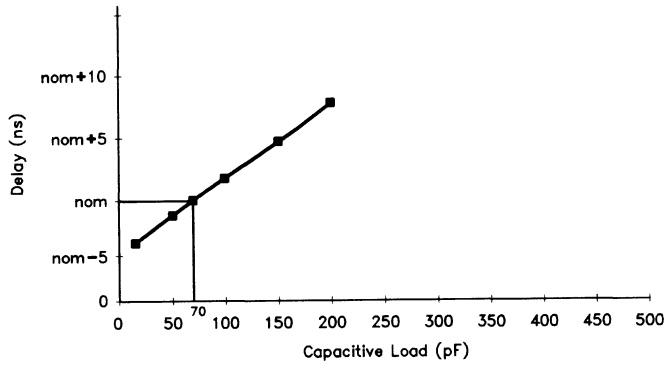
Type F

Capacitive Derating Curves (Continued)



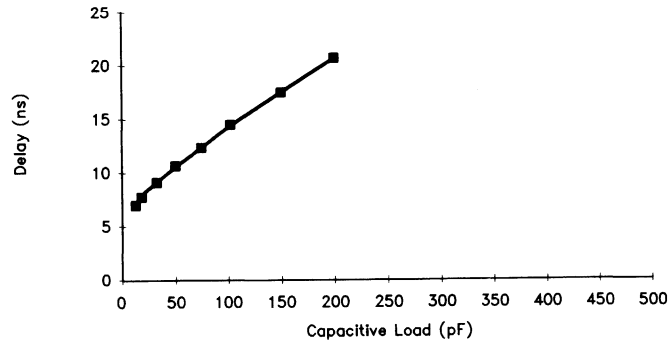
240814-76

Type G



240814-77

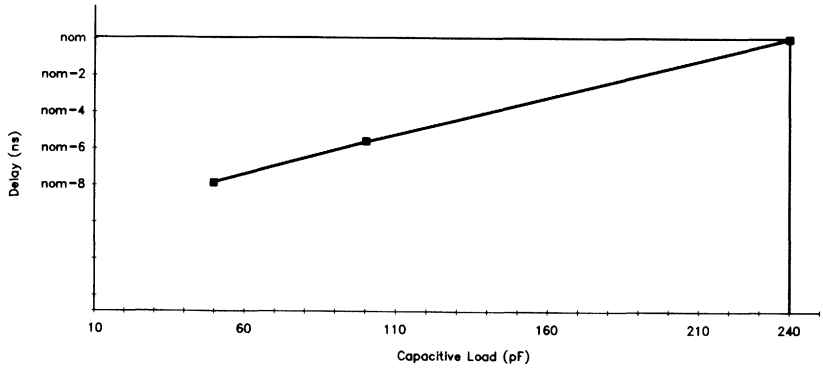
Type H



240814-78

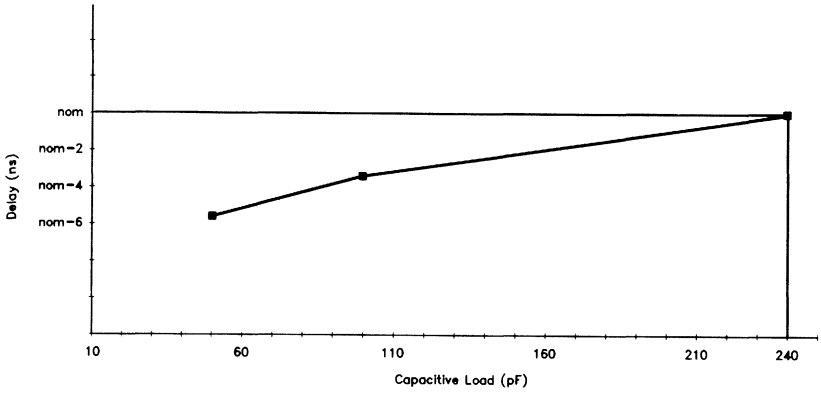
Type I

Capacitive Derating Curves (Continued)



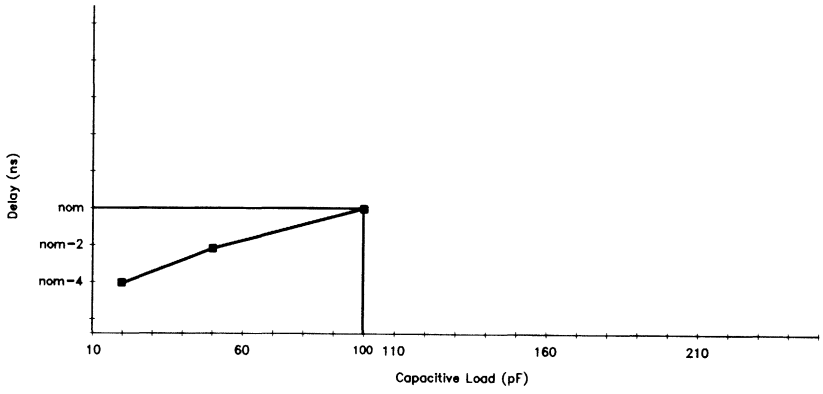
240814-79

Type J



240814-80

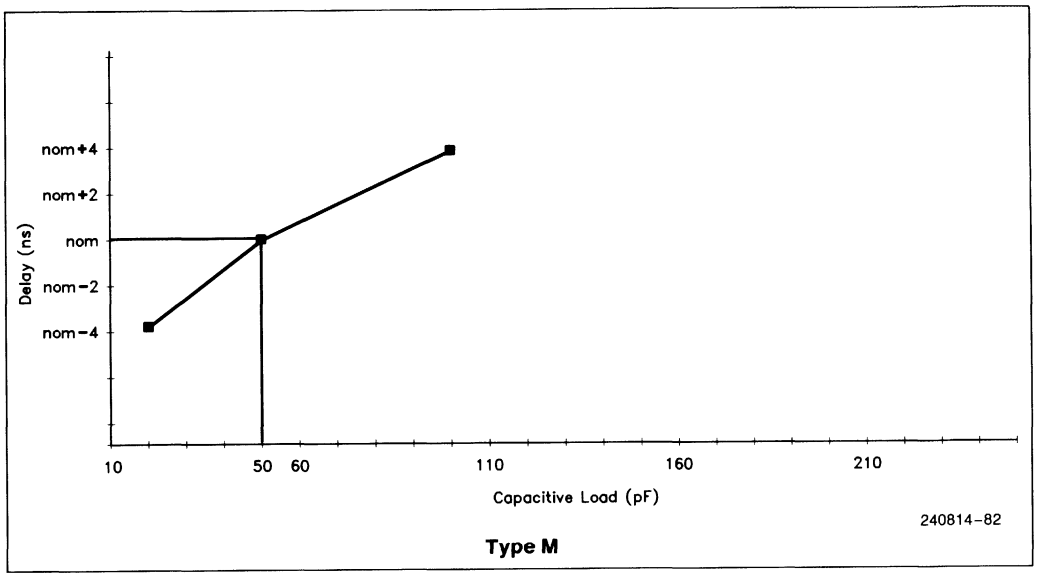
Type K



240814-81

Type L

Capacitive Derating Curves (Continued)



Type M

Capacitive Derating Curves (Continued)

9.0 DAMPING RESISTOR REQUIREMENTS

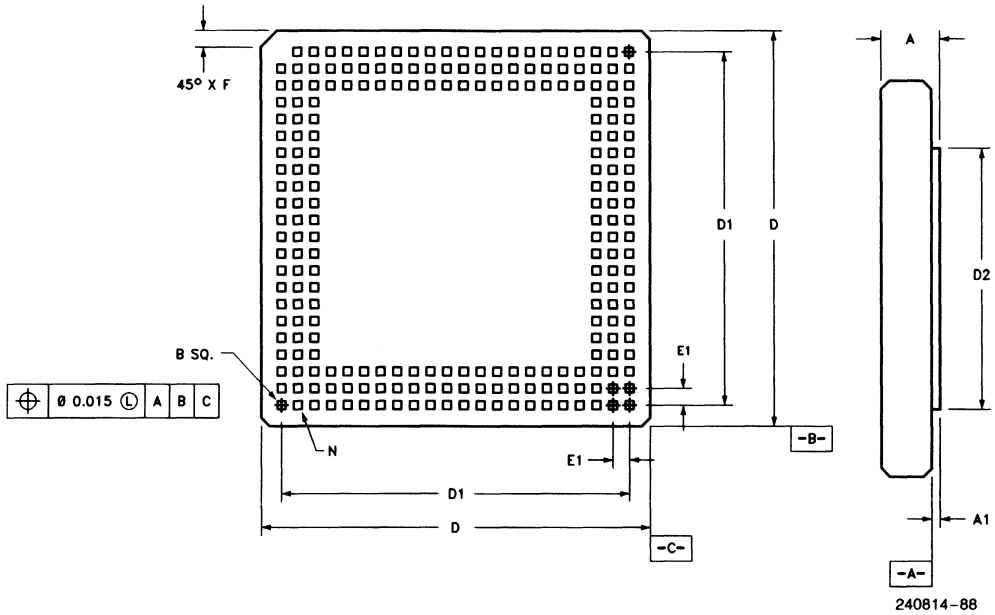
The SL SuperSet has powerful output buffers capable of directly driving large loads. These buffers are designed for fast signal transition times and hence have low output impedence. Due to a mismatch between the output impedance of the buffers and the characteristic impedance of the load (trace capacitance and the total number of devices) voltage overshoot and ringing can occur at signal transitions. By matching the output impedance with the characteristic input impedance and avoiding long trace lengths, the system designer can minimize the transmission line reflections and ringing.

The ringing at signal transitions of address and data lines cause long unstable periods. Ringing on control signals can cause false latching. To minimize the ringing effect series damping resistors may have to be connected. For additional hardware system design information, consult see the 386™SL Microprocessor SuperSet System Design Guide (Intel Order # 240816).

10.0 MECHANICAL DETAILS OF LGA AND PQFP PACKAGES

This section contains mechanical details of the two types of packages used in the SL SuperSet to help design the parts in. For more detailed information on packages and package types, please refer to *"Surface Mount Technology Guide"* (Order #240585)

227L CERAMIC LAND GRID ARRAY (CAVITY UP)



Family: Ceramic Land Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
1	3.56	4.06		0.097	0.120	
A1	0.33	0.43		0.009	0.017	
B	0.69	0.84		0.027	0.033	
D	28.96	29.46		1.140	1.160	
D1	26.67		Basic	1.050		Basic
D2		24.13			0.950	
e1	1.27		Basic	0.050		Basic
F	1.65	2.16		0.065	0.085	
N	227			227		
Issue	4/17/90					

Figure 10-1a. Principal Dimensions of the 386™SL CPU in a 227-Lead LGA Package

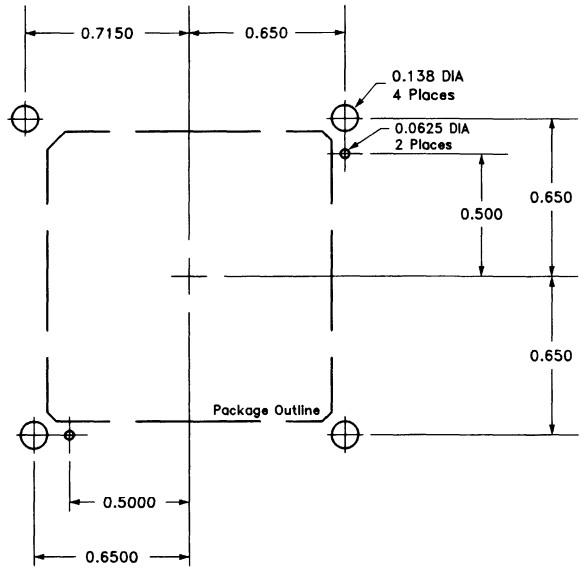
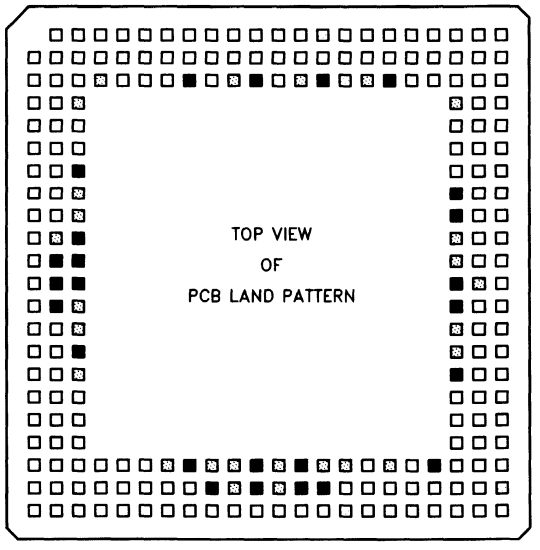
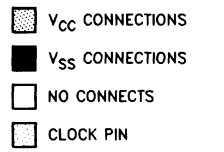


Figure 10-b. Recommended LGA Socket Footprint





- All power pins can be routed towards the middle.
- Outer two rows route outward
- Clock pins should have shortest possible traces, then via to shielded inner layer.

Figure 10-1c. Recommended Signal Routing for LGA Package

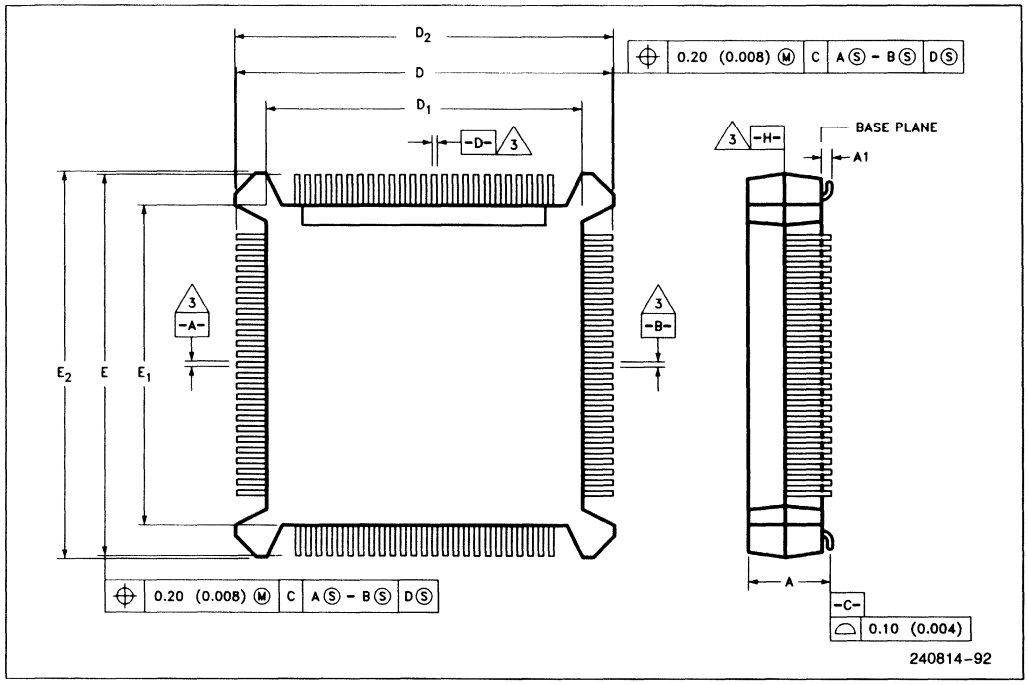


Figure 10-2a. Principle Dimensions of the 82360SL I/O in the 196-Lead PQFP Package

Family: 196-Lead Plastic Quad Flat Package (PQFP) 0.025 Inch (0.635mm) Pitch

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A = Package Height: Distance from seating plane to highest point of the body	4.06	4.32	0.160	0.170
A1 = Standoff: Distance from Seating Plane to Base Plane	0.51	0.76	0.020	0.030
D/E = Overall Package Dimension: Lead Tip to Lead Tip	37.47	37.72	1.475	1.485
D1/E1 = Plastic Body Dimension	34.21	34.37	1.347	1.353
D2/E2 = Bumper Distance	38.02	38.18	1.497	1.503
D3/E3 = Lead Dimension	30.48 Ref		1.200 Ref	
D4/E4 = Foot Radius Location	36.14	36.49	1.423	1.437
L1 = Foot Length	0.51	0.76	0.020	0.030

NOTES:
1. All PQFP case outlines are being presented as standards to the JEDEC.
2. Typical board footprint area for the 196-lead PQFP is 1.500 inches x 1.5000 inches.
3. All dimensions and tolerance conform to ANSI Y14.5M-1982.
4. Datum Plane -H- located at the molding parting line and coincident with the bottom of the lead where the lead exits the plastic body.
5. Datums A-B and -D- to be determined where the center lead exits the plastic body at datum plane -H-.
6. Controlling dimension in inches.
7. Dimensions D1, D2, E1, and E2 are measured at the molding parting line and do not include mold protrusions.
8. Pin 1 identifier is located within one of the two zones indicated.
9. Measured at datum plane -H-.
10. Measured at seating plane datum -C-.

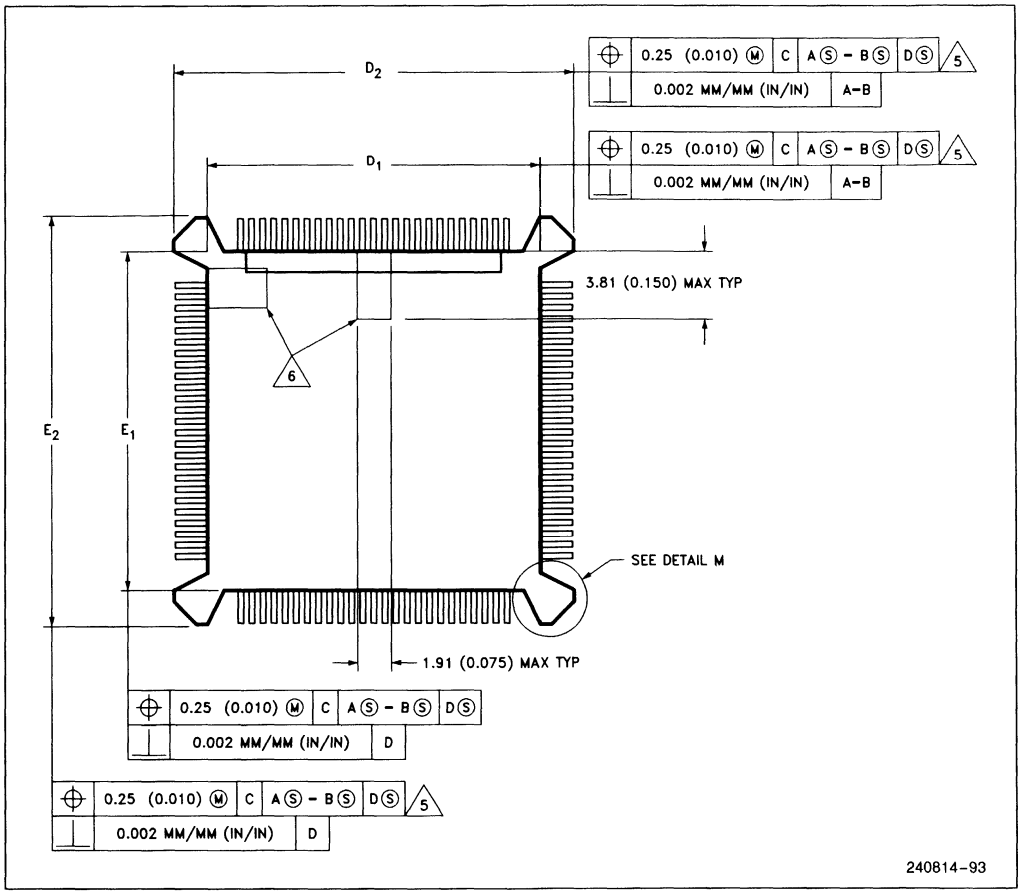


Figure 10-2b. Detailed Dimensions of the 82360SL I/O in the 196-Lead PQFP—Molded Details

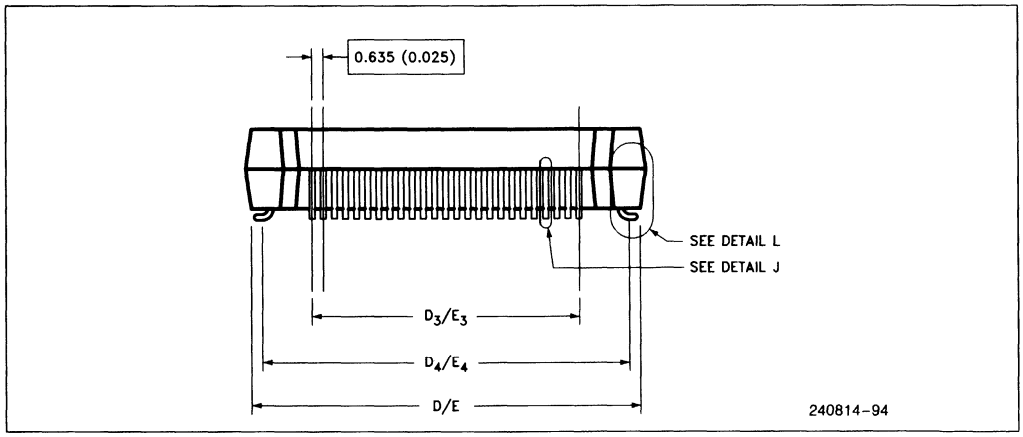


Figure 10-2c. Detailed Dimensions of the 82360SL I/O in the 196-Lead—Terminal Details

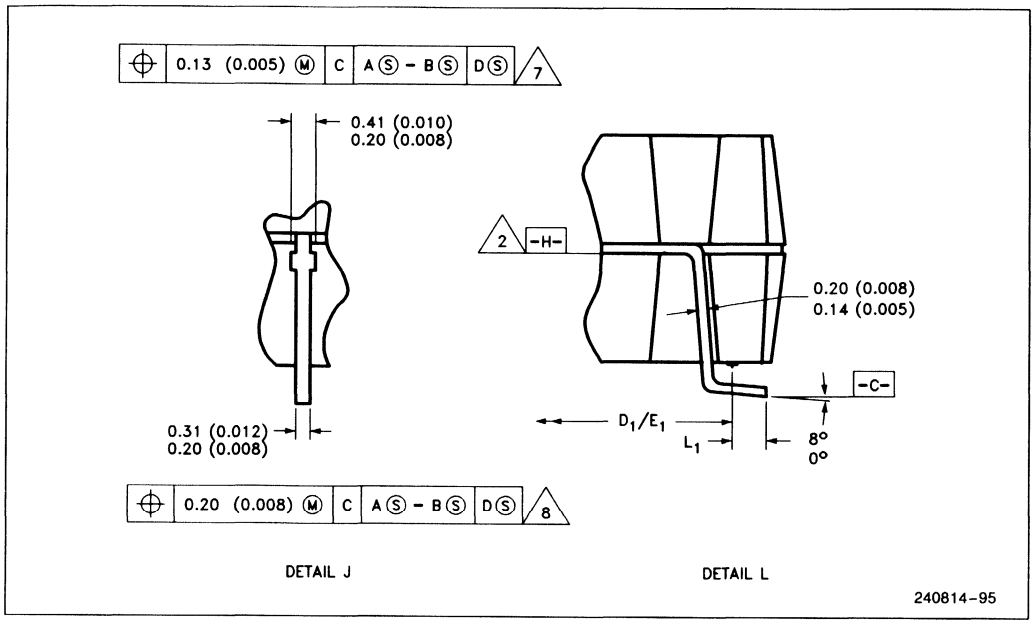


Figure 10-2d. 196-Lead PQFP Mechanical Package Detail—Typical Lead

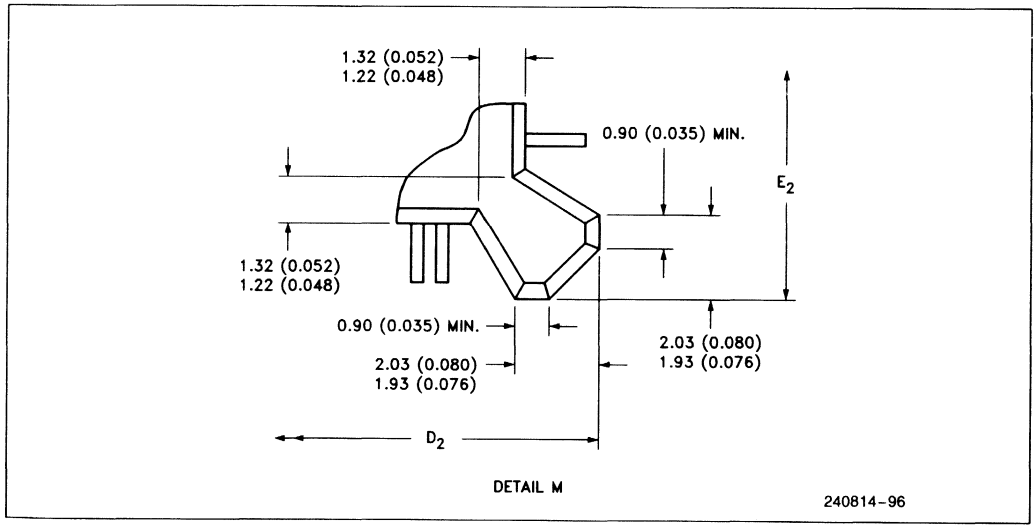


Figure 10-2e. 196-Lead PQFP Mechanical Package Detail—Protective Bumper

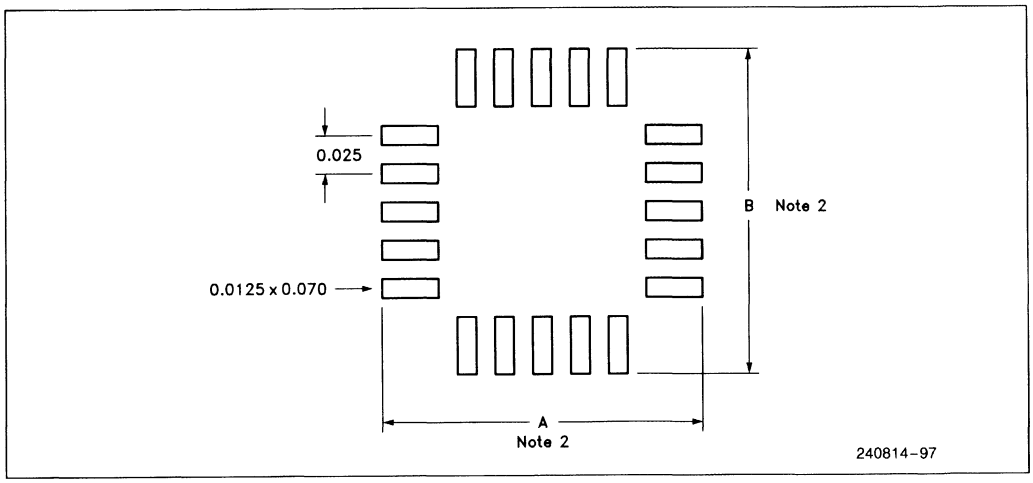


Figure 10-2f. Recommended PQFP Footprint

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The First Release of the Advanced Information Data Sheet reflects information believed to be accurate as of September 1990.

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Tel: 03 8900970
FAX: 03 8990819

BRAZIL

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Rua Geraldo Flausina Gomes, 78
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04575 - Sao Paulo - S.P.
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FAX: 55-11-534-9424

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Novel Precision Machinery Co., Ltd.
Room 728 Trade Square
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Tel: (852) 360-8999
TWX: 32032 NVTNL HX
FAX: (852) 725-3695

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Basavanagudi
Bangalore 560 004
Tel: 011-91-812-600-631
011-91-812-611-365
TLX: 9538458332 MDBG

Micronic Devices
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Swastik Chambers
Sion, Trombay Road
Chembur
Bombay 400 071
TLX: 9531 171447 MDEV

Micronic Devices
25/8, 1st Floor
Bada Bazaar Marg
Old Rajinder Nagar
New Delhi 110 060
Tel: 011-91-11-5723509
011-91-11-589771
TLX: 031-63253 MDND IN

Micronic Devices
6-3-348/12A Dwarakapuri Colony
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Tel: 011-91-842-226748

S&S Corporation
1587 Kooser Road
San Jose, CA 95118
Tel: (408) 978-6216
TLX: 820281
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JAPAN

Asahi Electronics Co. Ltd.
KMM Bldg. 2-14-1 Asano
Kokurakita-ku
Kitakyushu-shi 802
Tel: 093-511-6471
FAX: 093-551-7861

CTC Components Systems, Inc.
4-8-1 Dobashi, Miyamae-ku
Kawasaki-shi, Kanagawa 213
Tel: 044-852-5121
FAX: 044-877-4268

Dia Semicon Systems, Inc.
Flower Hill Shinmachi Higashi-kan
1-23-9 Shinmachi, Setagaya-ku
Tokyo 154
Tel: 03-439-1600
FAX: 03-439-1601

Okaya Koki
2-4-18 Sakae
Naka-ku, Nagoya-shi 460
Tel: 052-204-2916
FAX: 052-204-2901

Ryoyo Electro Corp.
Konwa Bldg.
1-12-22 Tsukiji
Chuo-ku, Tokyo 104
Tel: 03-546-5011
FAX: 03-546-5044

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J-Tek Corporation
3rd Floor, Samho Bldg.
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FAX: (822) 557-8304

Samsung Electronics
Samsung Main Bldg.
250, 2-KA, Taepyung-Ro
Chung-Ku, Seoul
C.P.O. Box 8780
Tel: (822) 751-3680
TWX: KORSST K 27970
FAX: (822) 774-7445

MEXICO

SSB Electronics, Inc.
675 Palomar Street, Bldg. 4, Suite A
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TLX: 287751 CBALL UR
FAX: (619) 585-8322

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Azcapotzalco
C.P. 02760-Mexico, D.F.
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TLX: 177 3790 Dicome
FAX: 52-5-561-1279

PHI S.A. de C.V.
Fco. Villa esq. Ajusco s/n
Cuernavaca – Morelos
Tel: 52-73-13-9412
FAX: 52-73-17-5333

NEW ZEALAND

Email Electronics
36 Olive Road
Penrose, Auckland
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FAX: 011-64-9-592-681

SINGAPORE

Electronic Resources Pte, Ltd.
17 Harvey Road
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FAX: (65) 289-5327

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FAX: 011-2712-803-8294

TAIWAN

Micro Electronics Corporation
12th Floor, Section 3
285 Nanking East Road
Taipei, R.O.C.
Tel: 886-2-506-3320
FAX: 886-2-719-7916

Acer Sertek Inc.
15th Floor, Section 2
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Taipei 10479 R.O.C.
Tel: 886-2-501 0055
TWX: 23756 SERTEK
FAX: 886-2-501 2521

*Field Application Location

CG/SALE/041090